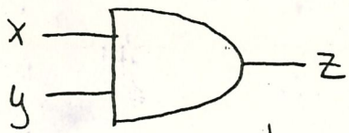
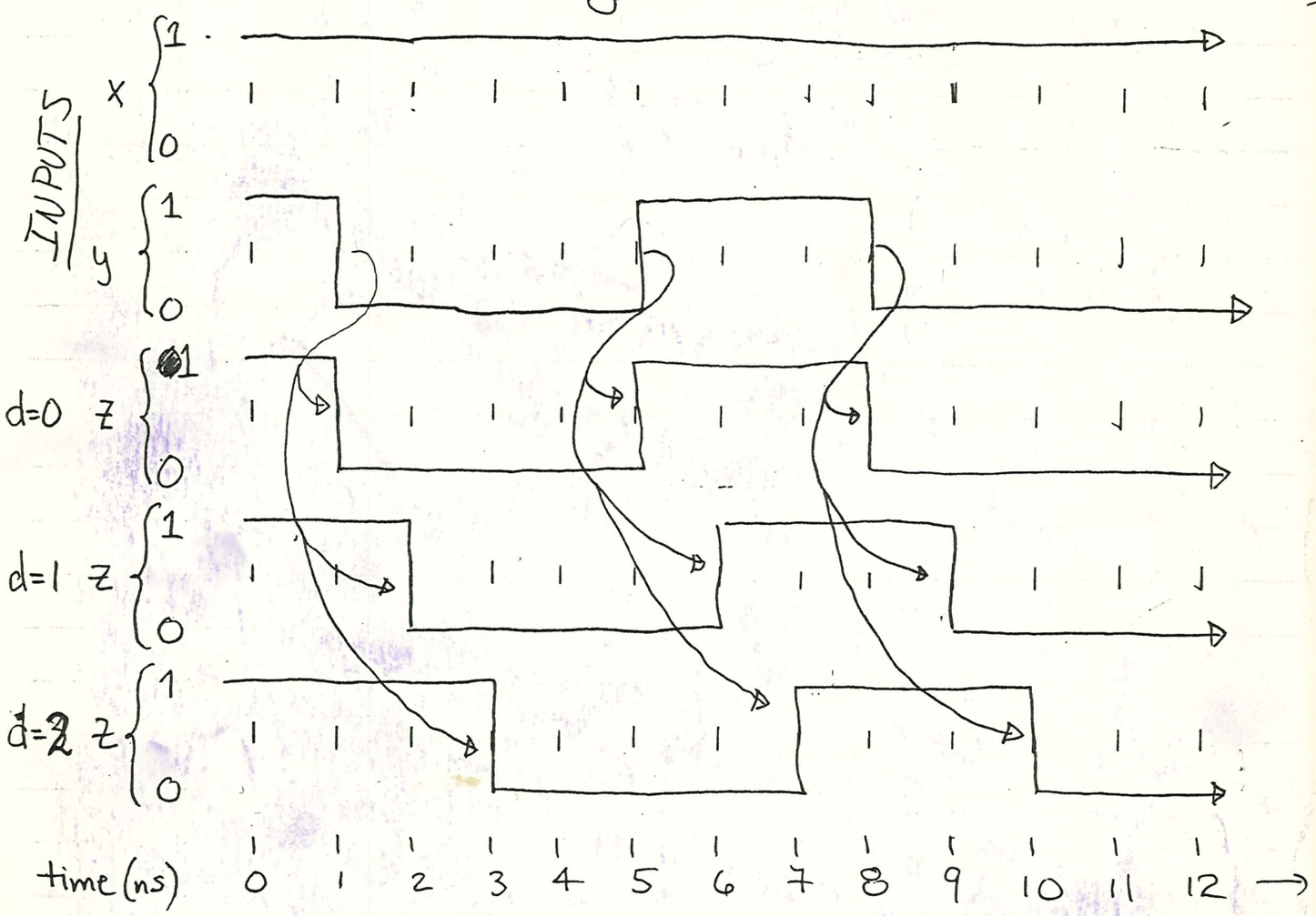
COT 3132 Timing Diagrams and gate delays.

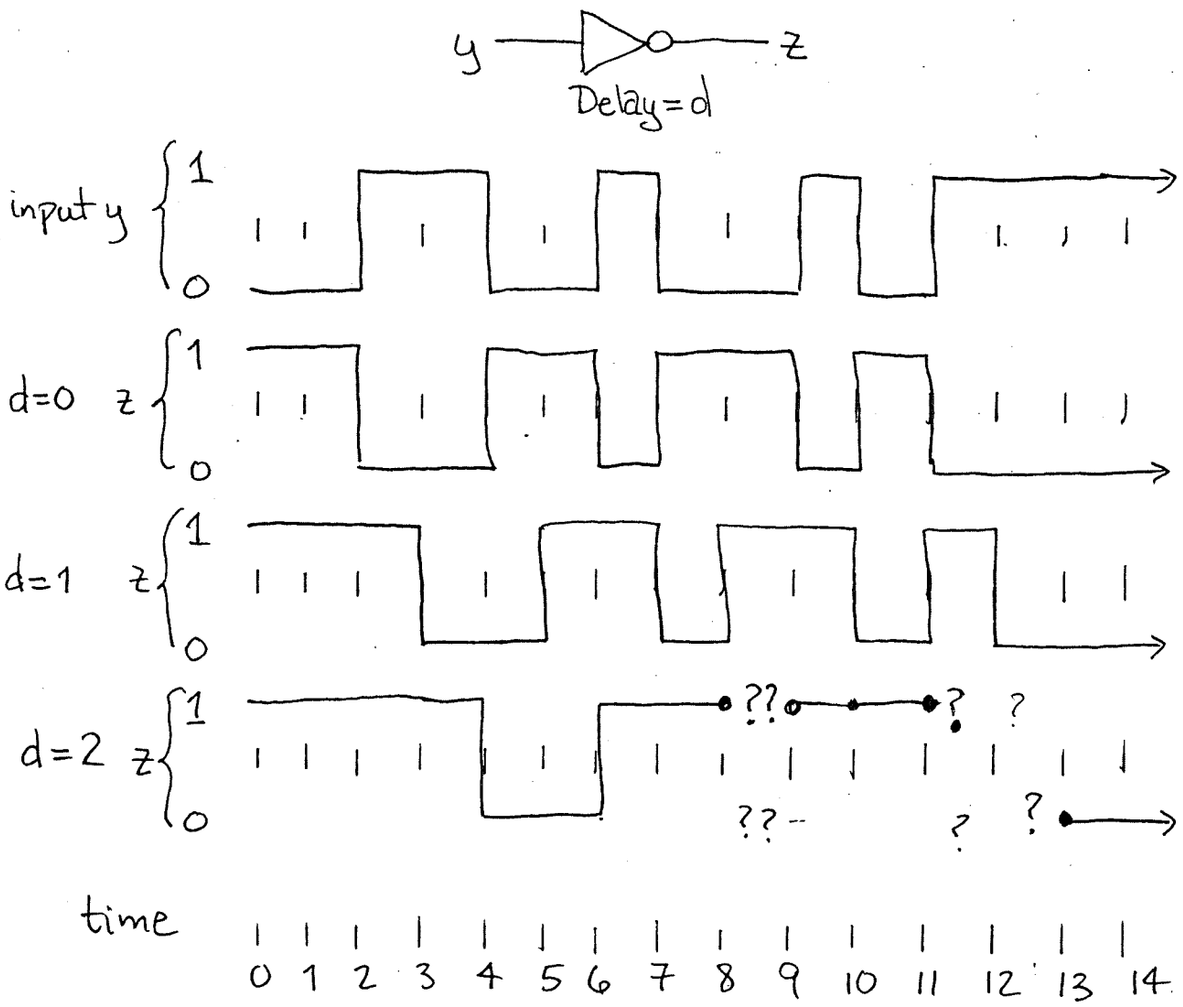


Delay = d ns (ns ≐ nanoseconds = 10^{-9} sec)



With a delay d=0, the output immediately reflects the change of input. This is shown on the third line labeled d=0. With a delay of d=1 ns the output is shifted one unit to the right. That is it takes the signal "y" to take one nanosecond to get through the gate. This is the line labeled d=1. The line d=2 shows what happens when d=2 ns.

Note the arrows which point ~~the~~ from what caused what. Clearly having delays makes our model more realistic. Unfortunately, there are problems with it. For example.



Clearly something different is happening between t=8 and t=9 (and between 11 & 13) when the delay is 2 ns. Note that the pattern doesn't just pass right on through. It takes a certain amount of energy to make a gate change. The period y=1 between t=6 to t=7 may not have enough to make the output change or then again it could. To be truely realiztic would make things to complex. Thus we assume

The inputs must be & remain steady through the <u>whole</u> delay time in order for the output to change. Otherwise, the output is undetermined.

Note that by t=9, y=0 for 2ns so there is no question about the gates output until t=11.

In the real world the following factors must be included.

1. gates can have different delays going from 0 to 1, than going from 1 to 0.

2. the delay time can change for the same gate depending on things like temperature.

3. different inputs can have different delays.

4. the change from 0 to 1 takes a certain amount of time and passes through intermediate values.

5. it is possible for gates to output values different from 0 or 1 if you confuse its inputs enough.

6. different gate technologies provide different delays for the same "type" (i.e. And, Or, etc) of gate.

7. external elements in the same circuit can effect gate speed (capacitors, etc).

8. gates age.

9. Enough!