

Digital Practice Test (PT-1)

- Two 8-bit registers have $(8C)_{16}$ and $(F9)_{16}$ resp. hex contents. What is the out come in hexadecimal if they are "XOR"ed?
- Define "single error detecting codes" and state what is meant by a minimal Product of sums form of a switching function.
- Simplify the boolean alg exprs $x+y'+(x+y'+z)'$ & $xy+(x+z)'+yz$
- Show in any boolean alg $a \leq b$ & $b \leq c \Rightarrow a \leq c$ [$a \leq b \Leftrightarrow a \cdot b = a$]
- Prove that { NAND } is functionally complete.
- Draw a map for the function $f(x,y,z)$



- For $\sum (0, 2, 4, 5, 6, 8, 10, 12)$ find all the prime implicants which are essential? Give a minimal sum of products form for f . Is it unique?

8. Prove or disprove $xy + x'y + x'z + yz = xy + xy' + x'z + yz$

- $f(w,x,y,z) = \sum (0, 2, 4, 9, 12, 15) + \sum \phi (1, 5, 7, 10)$

AB give a min. sum of prod.
 CD give a min. prod of sum
 E1 is the ans in AB unique? (Y/N)
 E2 is the ans in CD unique? (Y/N)
 E3 which is minimal (Neither, AB, CD, or both)

10. Show that $f(x,y,z) = (x'+y)z'$ is functionally complete

11. Show for any boolean alg. $x \oplus (y \oplus z) = (x \oplus y) \oplus z$ and $x \oplus (x \oplus y) = y$

12. Prove by induction for $n \geq 2$ (in any boolean alg)

$$\underbrace{x \oplus x \oplus \dots \oplus x}_n = \begin{cases} 0 & \text{if } n \text{ is even} \\ x & \text{if } n \text{ is odd} \end{cases}$$

13. Give a minimal two level AND-OR realization of the function in #6 above

14. Explain why the following yields a min prod of sums form for f

- Map f
- Complement the map
- Find min sum of prod form for the new map
- Complement ans in 3

15. Will the code 0110, 1001, 1111, 1100, 0011 detect single errors? why or why not?

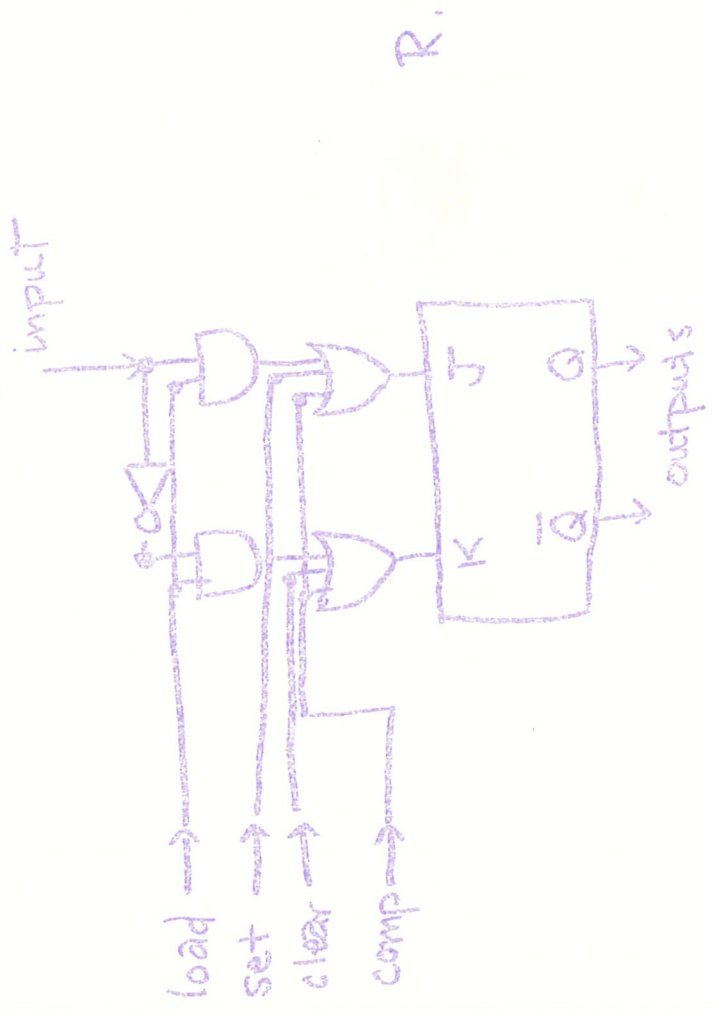
16. For any boolean alg define $A \oplus B = B + A'$
 prove or disprove $A \oplus B = B \oplus A$.

1-bit register R.

R has two outputs (Q, \bar{Q}), one input (for load) and four control lines (CLEAR, SET, LOAD, COMPLEMENT). R satisfies the following table

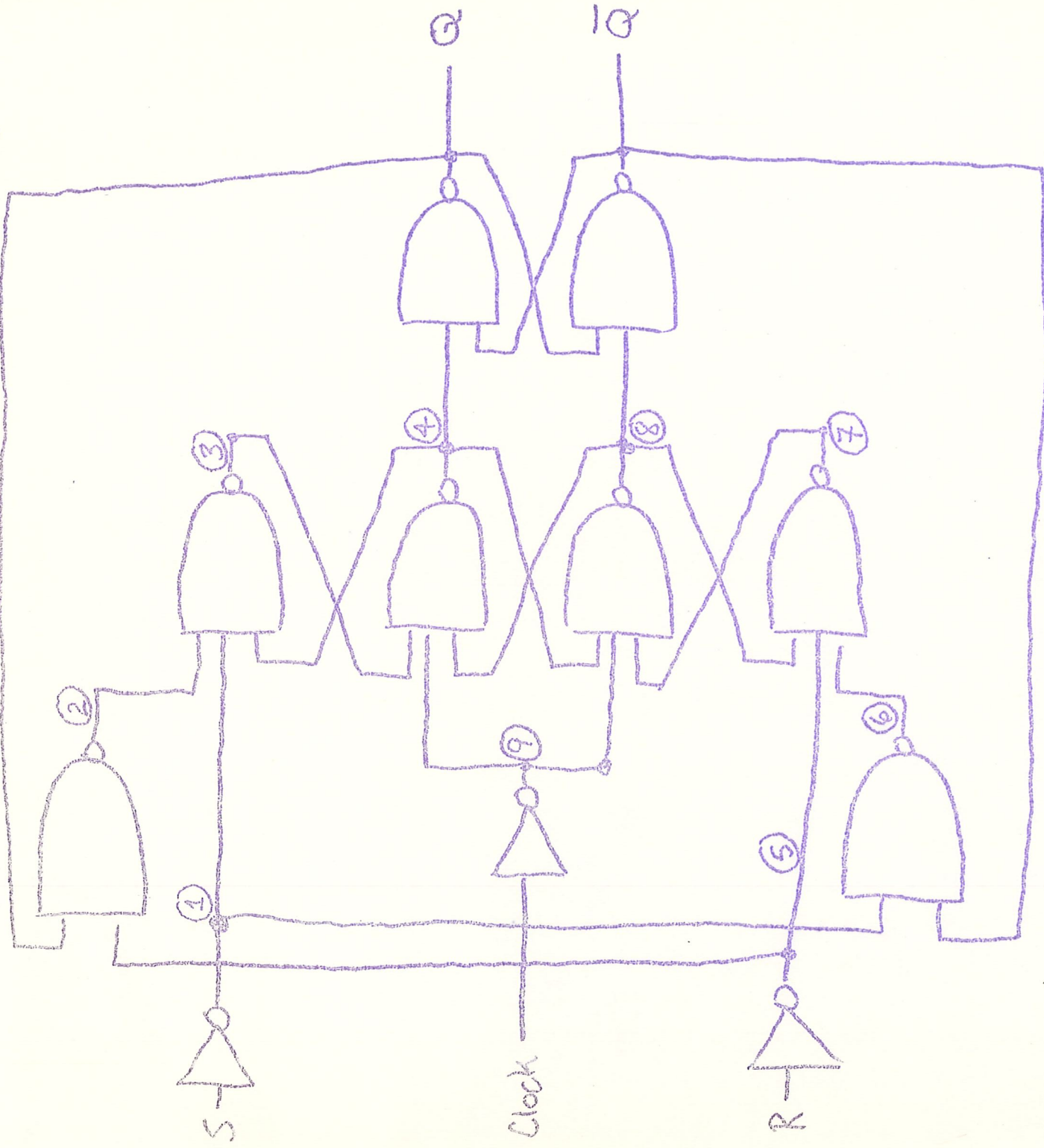
input	control inputs				current state	next state
	clear	set	load	compl.		
y	0	0	0	0	Q	Q
y	1	0	0	0	Q	0
y	0	1	0	0	Q	1
y	0	0	1	0	Q	y
y	0	0	0	1	Q	\bar{Q}
y	← all others →				Q	? (doesn't matter)

For example R could be realized using a JK flip flop via the following circuit



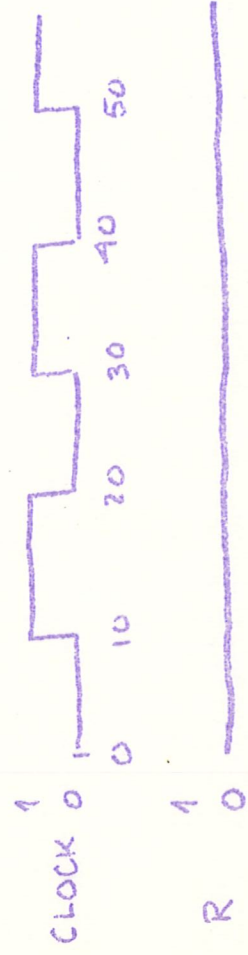
YOUR PROBLEM: WITHOUT putting any gates on the clock line NOR using preclear or preset, realize the 4-bit register R

A. with a D flip flop
 B. with a T flip flop

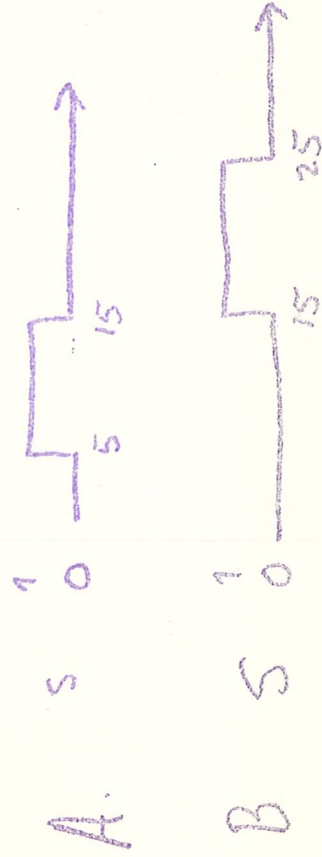


ALL GATES HAVE DELAY OF ONE ns

initially $R = S = \text{CLOCK} = Q = \bar{Q} = 0 = 0 = 0 = 0$
 $\bar{1} = 5 = 9 = \bar{Q} = 2 = 7 = 4$

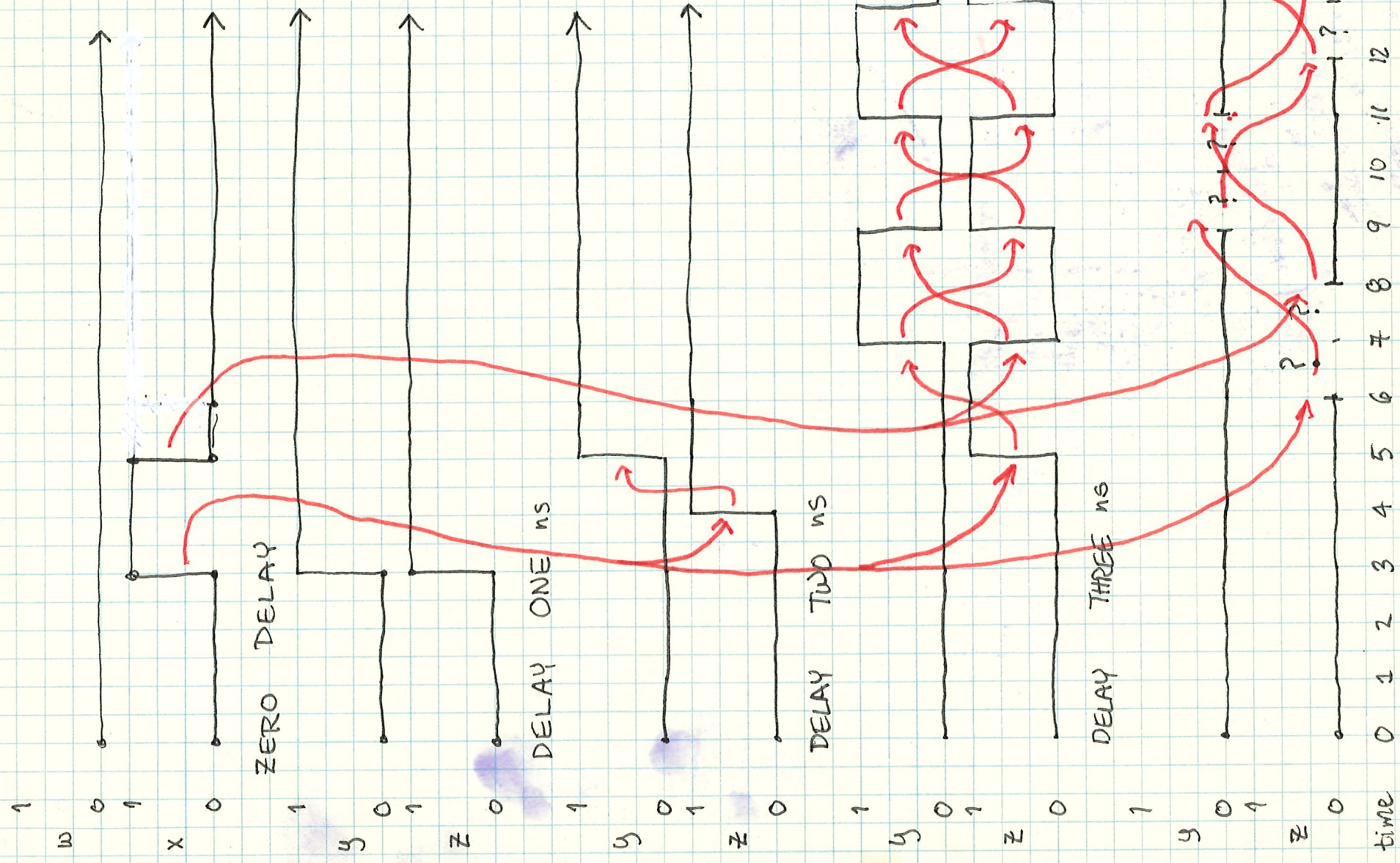


DO TIMING DIAGRAMS FOR BOTH CHOICES OF INPUT S





time 0 1 2 3 4 5 6 7 8 9 10 11 12 (in Nano Secs)

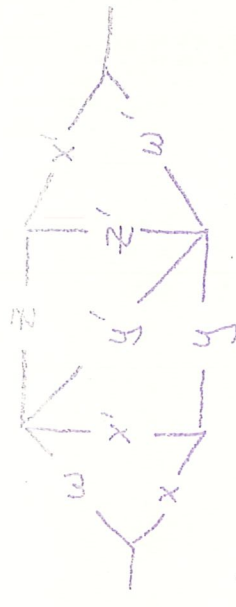


inputs

repeats forever

repeats forever

1. A. Find all the tie sets & cutsets for the contact network to right.
- B. Give a map of the function
- C. Find an equivalent series parallel network



2. Assuming there is at most one error in the hamming code 1110010

A. Circle the bit in error or say there is none B. decode the message.

C. Encode "5" in hamming code



3. Give a map for the threshold unit to right
 B. Use our technique for map entered variables on the map to right.

0	A	0	0
0	1	1	B
0	A	0	0
0	0	B	0

4. Use 3 2x4 decoders with enable to make a 3x8 decoder with enable

B. Use a 3x8 decoder and an or gate to realize $f(x,y,z) = x \oplus y \oplus z$

C. Do the same for port (B) with a 8x1 multiplex unit

5. Give a state diagram which will recognize the sequence 010 (overlaps ok) ie if input $x = 100010100101010$ then output is $z = 00000101001000001$



6. do a time diagram for all gates have a delay of 1 ns.



$A = 0 \quad B = C = D = 1$ initially

7. Realize the state table using a JK flip flop

$x=0$	$x=1$
0/1	1/0
1/1	0/1

8. List the need^{ed} excitations

Change required	0 to 0	0 to 1	1 to 0	1 to 1
	U	K	B	R
			T	D

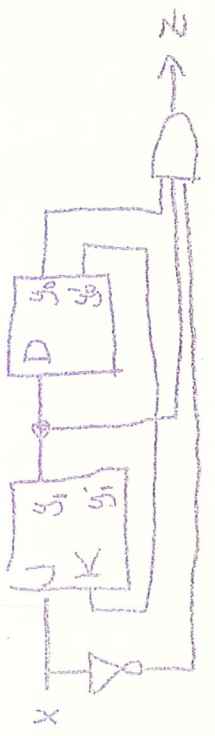
9. for prime implicant chart

- A. Which implicants are essential?
- B. Which implicants are in every minimal express
- C. which implicants are in no minimal express.

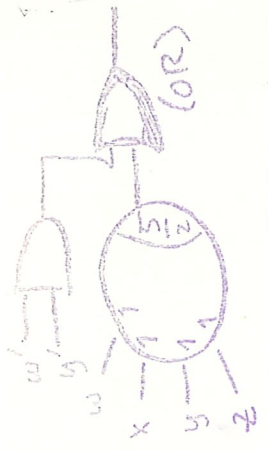
	a	b	c	d	e	f	g	h	i	j
A	x									
B		x								
C			x							
D	x									
E				x						
F					x					
G						x				

10. Realize $f = x + y$ using only NAND gates, using only NOR gates.

11. Give a state table for the circuit to right



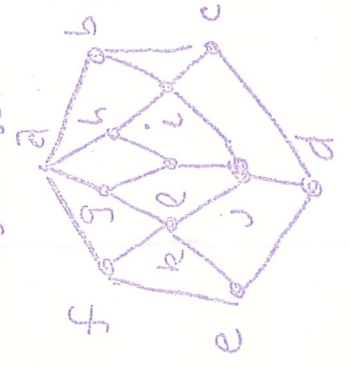
13 DIGITAL



- Find all static hazards in the map.
- In the circuit

Carefully step by step construct the equivalence partition and a state table in standard form for reduced

3. A Find All the Complements of e in the Hasse diagram



B. If $x = 101010$, $y = 100111$
 then gcb of $x \& y$ is _____
 and lub of $x \& y$ is _____
 (register order)

4. For each of the relations on $N = \{0, 1, 2, 3, \dots\}$

and Properties below either say yes or say no and give a counterexample
 xRy iff $|x-y| \leq 3$; xSy iff $x \leq y+3$

- is it reflexive B is it symmetric C is it anti-symmetric
- is it transitive E is it irreflexive

5. Use full (half) adders and a decoder to realize $S_{0,4,6} (x_1, x_2, x_3, \dots, x_7)$

6. Write $A S'_{1,2,3} (B, C, D, E) + A' S_{2,3,4} (B', C', D', E')$ as a symmetric function of A, B, C, D, E using the "S" notation

	x=0	x=1
A	A/0	D/1
B	B/0	C/1
C	D/1	A/0
D	E/1	B/0
E	F/0	G/0
F	A/0	H/0
G	A/0	D/1
H	B/0	C/1

7. A. Design a set-dominant unit using a RS flip-flop

S _d	R	current	next
0	0	Q	Q
0	1	Q	0
1	0	Q	1
1	1	Q	1

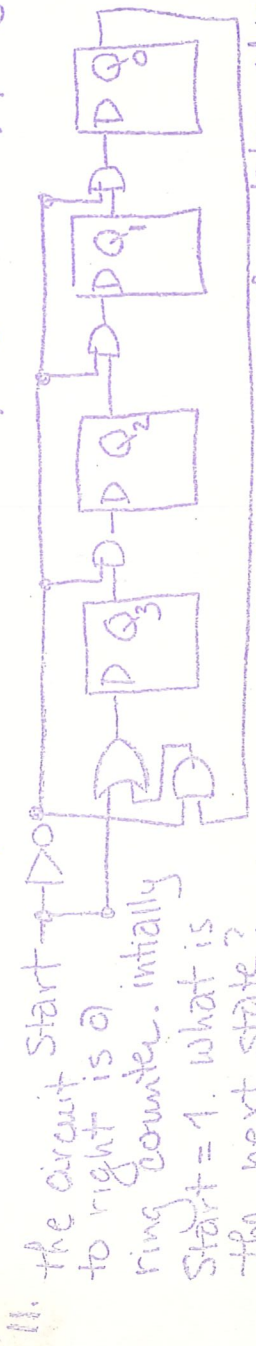
B. Use a set-dominant unit to realize a JK flip-flop

C. Design a unit using an RS flip-flop such that the '1' input is a hold otherwise it is the same as a RS flip-flop

8. The function $f(v, w, x, y, z) = \sum(8, 10, 13, 24, 28) + \sum \phi(A, 16, 17, 27, 31)$ has a decomposition of the form $F(w, z, \Phi(v, \dots))$. Find it.

- Design $S_{0,1,2} (w, x, y, z)$ using a contact network with a minimum of contacts
- Realize this same function using one threshold unit

10. Use contact networks with minimum of spring to realize $T(w, x, y, z) = \sum(6, 9, 11, 14, 15)$ [12 springs] Partial credit for circuits with more springs — if 4 springs started.



11. the circuit Start = 1 to right is a ring counter. initially Start = 1. What is the next state? After the first clock pulse Start = 0, list the states which follow in their order. Use two flip flops and a decoder to produce the same output sequence as $Q_3 Q_2 Q_1 Q_0$ (i.e. draw the circuit).

12. List all possible reduced state tables in standard form with 2 or less states where the output is always 0 when current state is A and always 1 when the current state is B

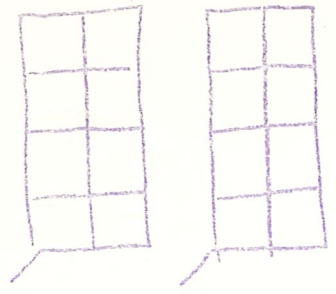
13. Design a 4-bit register with controls c_0, c_1 s.t. when $c_0=c_1=0$ it holds, when $c_0=1, c_1=0$ it counts up & when $c_0=0, c_1=1$ it counts by twos.

Show All Work for Credit 1-4; Opts ea. 5-8 15 pts ea.

1. A. "OR" the two 8-bit registers containing $(A3)_{16}$ and $(47)_{16}$ and express the outcome in hexadecimal.

B. Define a single error detection code.

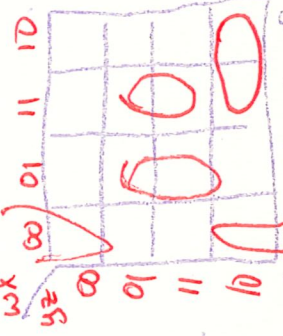
2. Prove or disprove: $x'z + yz + x'y = x'z + yz + xz$
(ANY Boolean Alg)



3. Prove for any boolean algebra $xy + [(x'z)'(w'y'+z)'] = xy + x'z$

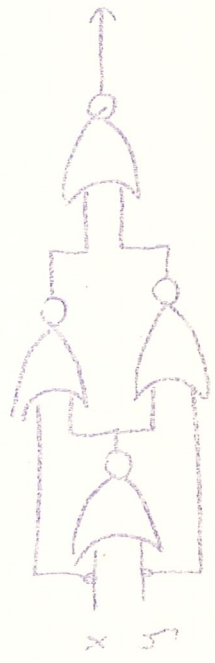
4. Show $f(x,y,z) = (x+y)z'$ is functionally complete

5. A $f(w,x,y,z) = w'xy' + x'y'z' + y'z$ realize f as a two level circuit using only AND or OR gates. (primed variables avail.)



B. Draw a map for f in part A.

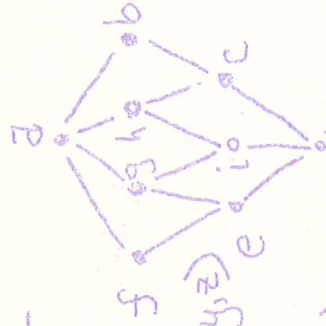
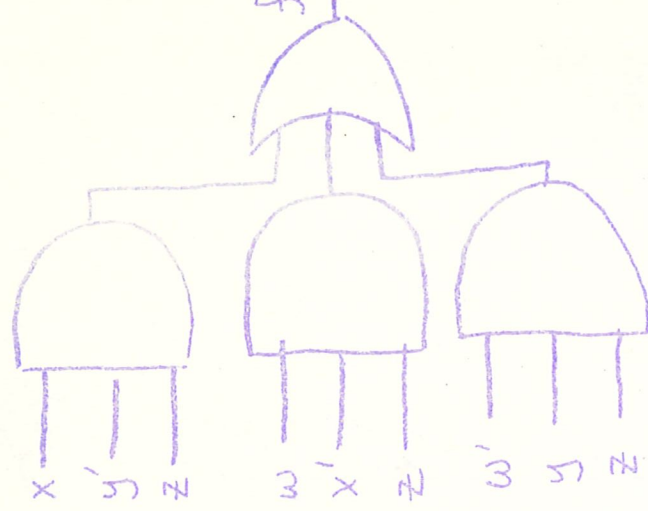
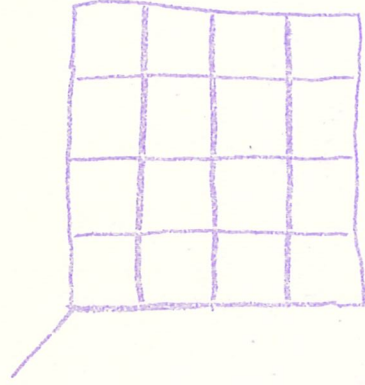
C. Write the output of the circuit below in a sum of products form



Show all work for Credit 1-4 10pts each 5-8 15pts each

1. A. Indicate All static hazards in the circuit to the right in the map beside it.

B. List All complements to e in the Hasse diagram to the right



2. The function $f(w, x, y, z) = \sum(1, 15, 20, 21, 27) + \sum\phi(4, 10, 11, 19, 26)$

has a decomposition of the form $F(w, y, \Phi(v, x, z))$. Find it.

3. The relation R is defined on $\{1, 2, 3, \dots\}$ by $xRy \iff x$ divides $2y$ with no remainder. For each property below either claim R has that property or claim R does not have that property and give an example to show it doesn't

A. Reflexive

B. Symmetric

C. Antisymmetric

D. Transitive

4. The function $AB S_3(C, D, E) + AB S_0(C, D, E) + A S'_{2,3,4}(B, C, D, E)$ is a symmetric function of A, B, C, D, E . Write it using the S notation

5. A. Rewrite the state table to right in standard form

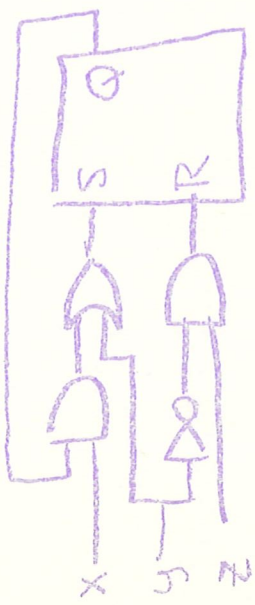
	x=0	x=1
A	C/0	A/0
B	A/0	B/1
C	C/1	D/0
D	A/1	B/1

BCD Carefully "Step by Step" construct the equivalence partition for the state table to the right. Show ALL work.

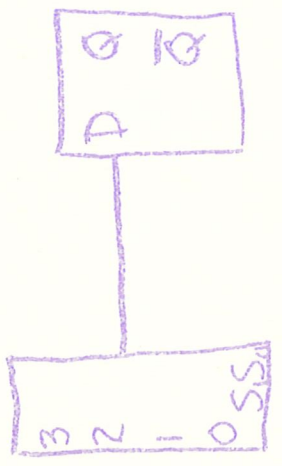
	x=0	x=1
A	C/0	E/0
B	D/1	F/1
C	E/0	G/0
D	F/1	H/1
E	G/0	G/0
F	H/1	B/1
G	G/0	B/0
H	B/1	D/1

E. Give a minimal length sequence that distinguishes state C from state E.

6. AB. Fill in the action column of the table to right for the circuit below. HOLD, SET, CLEAR, COMPLEMENT AND FORBIDDEN are "ACTIONS"



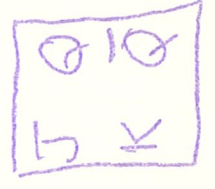
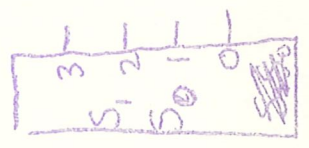
C. Use the D flip-flop below and the multiplexer to obtain



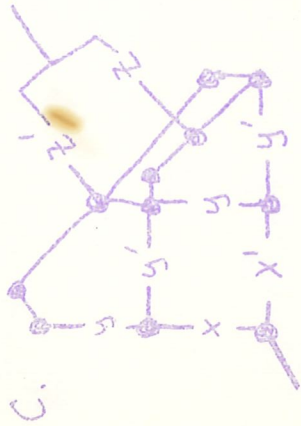
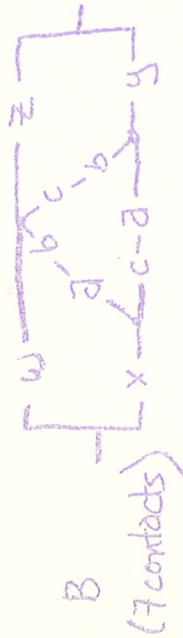
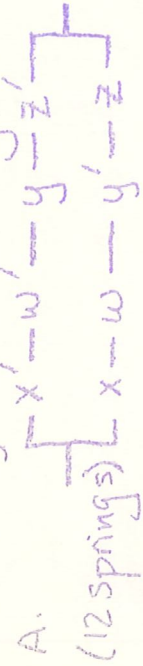
x	y	z	ACTION
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

S ₁ S ₀	ACTION
00	HOLDS
01	COMPLEMENTS
10	SETS
11	CLEAR

D. Use the decoder and JK flip-flop and no more than two gates to obtain



7. Simplify the following contact networks



(2pts for 8 springs
more for less)

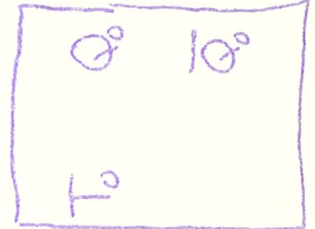
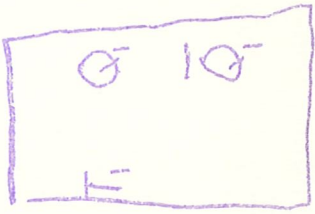
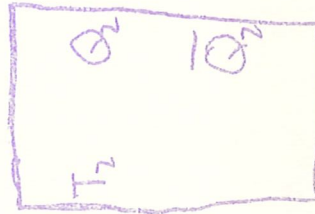
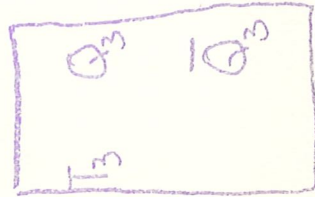
also below

8. Using the T-flip flops below and the control line C_n to realize a circuit which does $\rightarrow C$

Current State	Next State
0	$Q_3 Q_2 Q_1 Q_0$
1	$Q_3 Q_2 Q_1 Q_0$

Where $\{Q_i$ if $Q_{i-1} Q_{i-2}, \dots, Q_0$ are all zero
 $P_i = \{Q_i$ otherwise (i.e. if there is a one anywhere to the right)

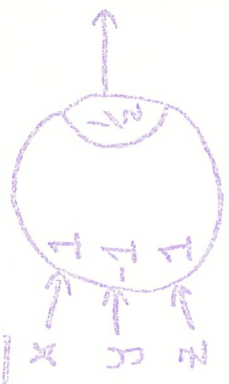
Control Line C _____



by DIGITAL by 1-4 worth 10pts 5-8 worth 15pts

1. The Hamming Code is used to send a decimal number and the following was received: 110000

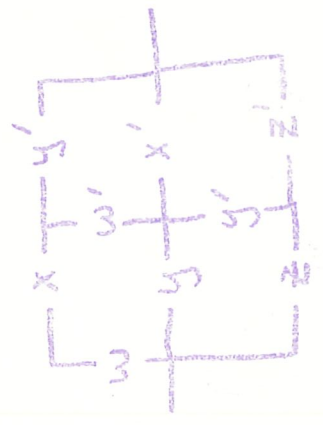
- A. Assuming at most one error either CIRCLE the bit in error above or SAY there is no error.
- B. What is the decoded message? _____



C. xy Fill in map below for the threshold unit on right



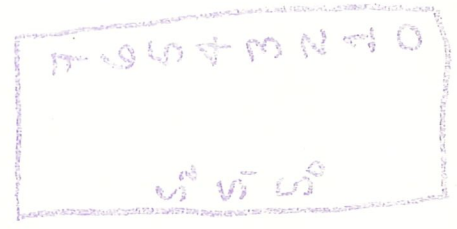
2. For the contact network to right



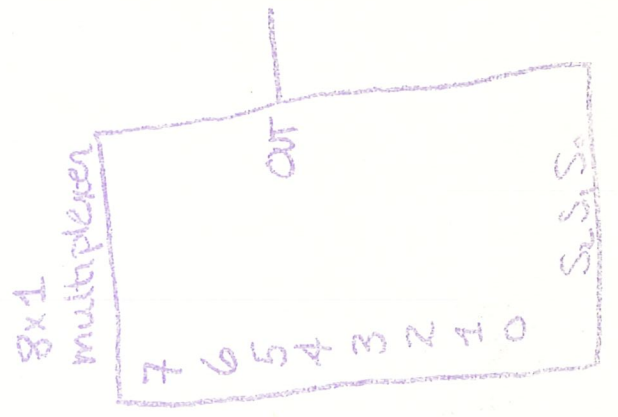
B. List all cut sets

3. CAREFULLY showing ALL work use the TABULATION method to find all prime implicants of $f(x,y,z) = \sum(3,4,5,6,7)$
Do NOT construct a prime implicant chart.

4. Realize the function $g(x,y,z) = \sum(3,5,6,7)$ using
A. The decoder & another gate B. The multiplexer



3x8 decoder



8x1 multiplexer

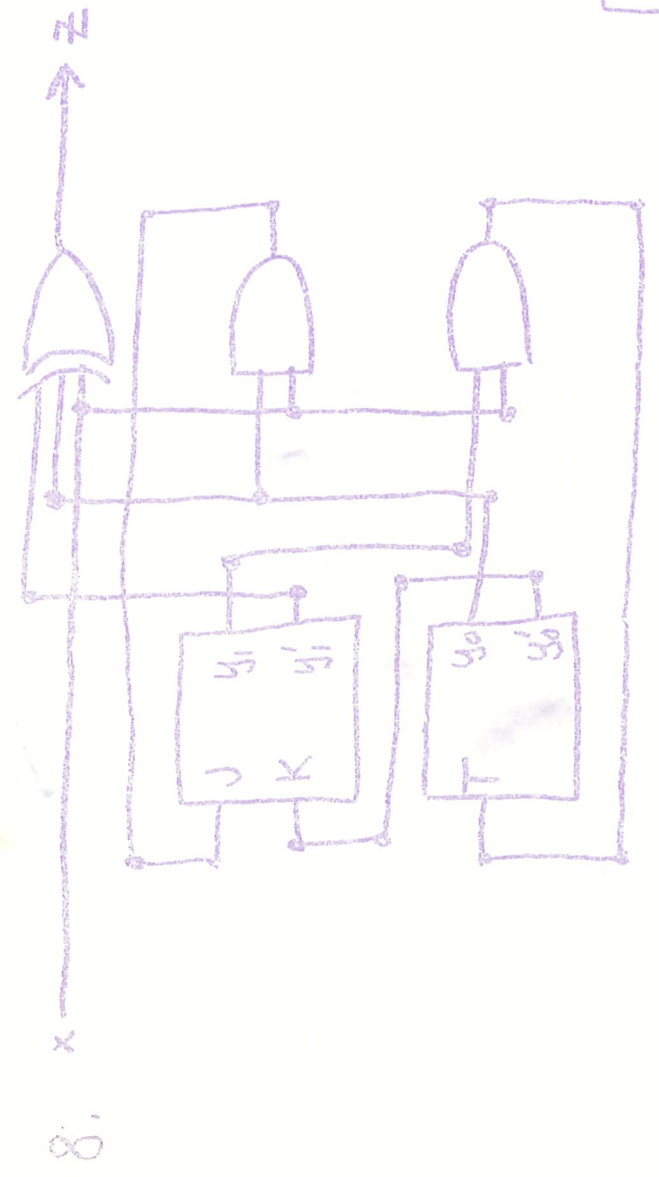
5. Complete the timing diagram below. Both gates have a delay of one nanosecond. Be sure to include ARROWS



6. Realize the state table below using an RS flip flop and other gates as needed

CURRENT STATE	NEXT STATE / OUTPUT	
	X=0	X=1
0	0/0	1/1
1	0/1	0/1

7. Give a state DIAGRAM which will recognize the sequence 000 and the sequence 11 (overlaps ok) i.e if $x = 0010000111$ clearly label which state you start in then $z = 0000011011$

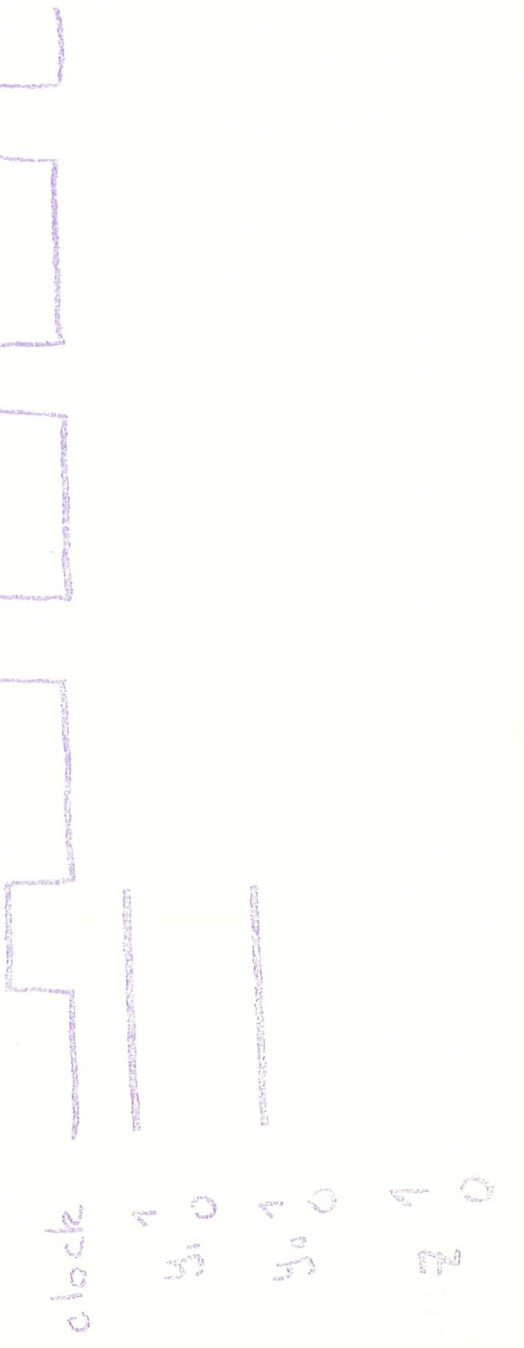


[Flip Flops are negative edge triggered]

A. Complete the state table below

CURRENT STATE $y_1 y_0$	NEXT STATE / OUTPUT	
	$x = 0$	$x = 1$
00		
01		
10		
11		

B. Suppose x is always 1 complete the following



The Old Digital Problem

- 1-8 40 pt each
- 9-16 15 pt each

1. For the circuit:



A. Give all the truth table entries.

B. Give all the output values.



2. A. Find all the prime implicants in the Karnaugh map.

B. Write the minimal sum-of-products the base 10 number for each.

3. Using one "or gate" and one "and gate" and "not gates" write the function of the circuit below. (Assume both printed variables are available.)

4. Give the minimal expression for the circuit. Give the minimal changes in the output.

CHANGE	INPUTS	OUTPUT
0 to 0	0 0	0
0 to 1	0 1	0
1 to 0	1 0	1
1 to 1	1 1	1

5. Find a minimal expression for the circuit with map reduction.

0	0	0
0	1	0
1	0	1
1	1	1

6. The relation R on $\{0, 1, 2, 3, \dots\}$ is defined by xRy if and only if $|x - y| \leq 3$. Answer yes or no and if no give an example which shows why.

A. is R reflexive? B. is R anti symmetric?

C. is R symmetric? D. is R transitive?

7. Show for ANY boolean algebra $x \oplus (x \oplus y) = y$
 $(x \oplus y) = xy' + x'y$

8. Show that $f(x, y, z) = (x' + y)z'$ is functionally complete.

9. $f(w, x, y, z) = \sum (0, 2, 4, 9, 12, 15) + \sum \phi (1, 5, 7, 10)$

AB. give a minimal sum of products form for f .

CD. give a minimal product of sums form for f

E1: Is your answer in AB unique? (Yes/No)

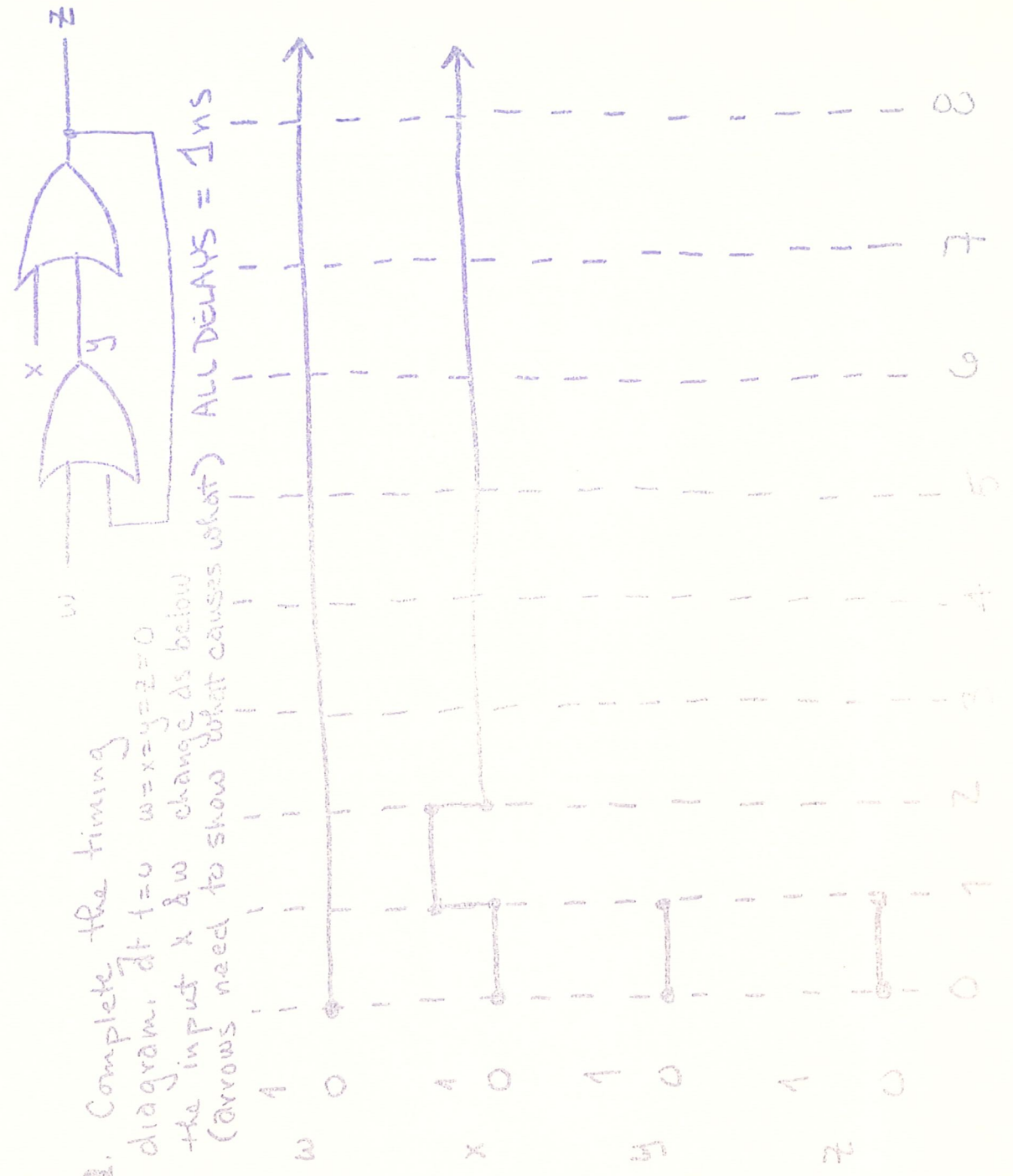
E2: " " " CD unique? " "

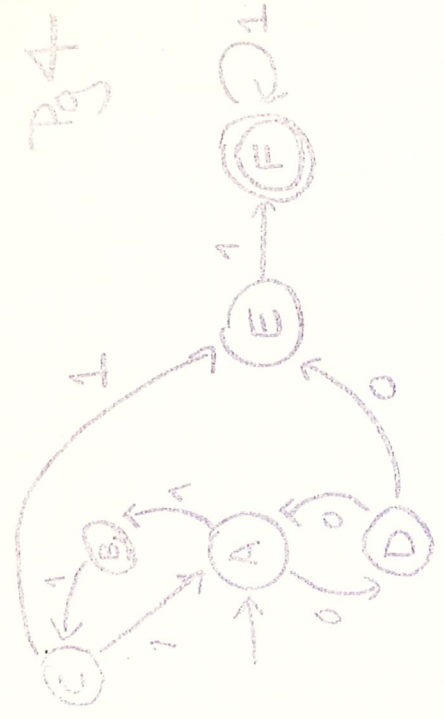
E3: which of these two answers is better?

10. Draw a transition graph for the sequence $1(11+0)^*1(11)^*(00)^*1$

11. Use full adders (half adders), ^{a decoder} and other things to realize $S_{0,4,6}^{(x_1, x_2, \dots, x_7)}$

12. Complete the timing diagram, at $t=0$ $w=x=y=z=0$ the input x & w change as below (arrows need to show what causes what)





13. For the transition graph
 A. Write a regular expression for the sequences accepted by it

B. Give a state table for an equivalent deterministic machine.

14. Realize the state table to right using a RS flip-flop and some gates

Current State y	Next state/Output x=0 x=1	
0	0/1	1/0
1	1/1	0/1

15. Design a way to hook any of the inputs x_i to any of the outputs z_j via the phone line. Call selects which x_i , $S_1 S_0$ selects which z_j

x_0 ---
 x_1 ---
 x_2 ---
 x_3 ---

--- telephone line ---
 (thanks to Ma Bell)

--- z_0 ---
 --- z_1 ---
 --- z_2 ---
 --- z_3 ---

$C_1 C_0$
 control

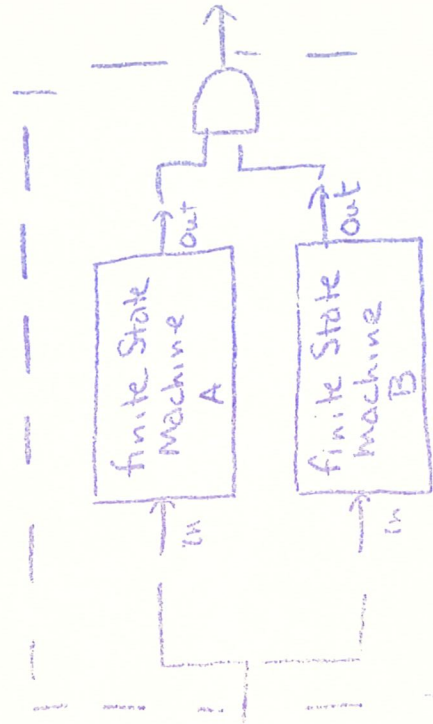
$S_1 S_0$
 control

i.e. $C_1 C_0 = 10$; $S_1 S_0 = 01$
 yields x_2 connected to z_1

16. The finite state machines A & B are physical, i.e. A has n flip-flops and B has m flip-flops plus some other gates.

A. What is the most number of states machine C can have?

BCDE. Explain how this can be used to prove if P and Q are regular expressions, then R_1 , the set of sequences accepted by both P & Q, is regular.



finite state machine C

Show all work for Credit
Good luck

1. Bif. $x = [101010]$ and $y = [100111]$

then A. glb of x & y is

--	--	--	--	--	--

 is

--	--	--	--	--	--

and B. lub of x & y is

--	--	--	--	--	--

 is

--	--	--	--	--	--

- CD Assume there is at most one error in the Hamming code 1110010
- C. circle the bit in error or say there is none.
- D. what is the message?



2. A. Fill in the map $\frac{xy}{z}$ for the function given by the threshold unit to right

B. Realize the map in 2A with a series-parallel network.

3. For the Prime Implicant chart to right, implicants A, B, & C have one less literal than D, E, & G. A which implicants are essential?

	a	b	c	d	e	f	g	h	i	j
A	x		x		x					x
B			x							
C										
D	x	x						x	x	
E					x					
F							x			
G										x

B. which non-essential implicants are in any minimal expression?
C. which implicants are never used?

4. The relation R on the set $N = \{0, 1, 2, 3, \dots\}$ is defined by xRy if and only if $x \leq y + 3$. Answer yes or no to the following & if your answer is no give an example that shows it following

- A. is R reflexive?
B. is R symmetric?
C. is R anti-symmetric?
D. is R transitive?

1-8 10pts each 9-16 15pts each.

1. A. "XOR" the two 8-bit registers containing (A3)₁₆ and (47)₁₆ and express the outcome in hexadecimal.

B. For the same register pairs express their g.l.b. in hexadecimal.

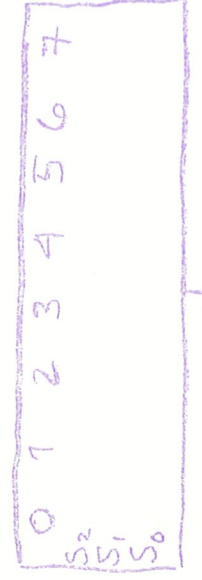
2. A. Encode 6 into Hamming code

B. The function $S_{2,3,4,5}(v, w, x, y, z)$ can be realized using one threshold unit. Do it.

3. A. Use our technique for map entered variables to find a minimal expression for the map \rightarrow

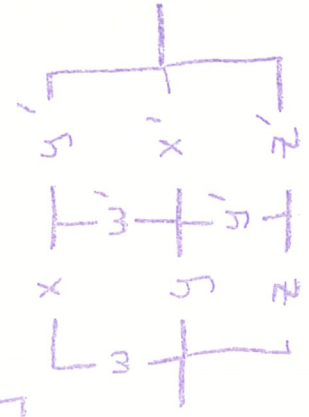
B. Use this 8x1 multiplexer to realize this map.

xy	0	A	A	0
z	B	∅	1	A'



4. For the contact network to right

- A. List all the sets
- B. List all cutsets



5. The function $A S_{0,2}(B', C', D', E') + A' S_{1,2,4}(B, C, D, E)$ is a symmetric function of A, B, C, D, E. Write it using the S notation.

6. The relation R is defined on $\{1, 2, 3, \dots\}$ by $xRy \Leftrightarrow x-y=3$. For each property below either state R has that property OR state that it doesn't have the property and give an example to show it doesn't.

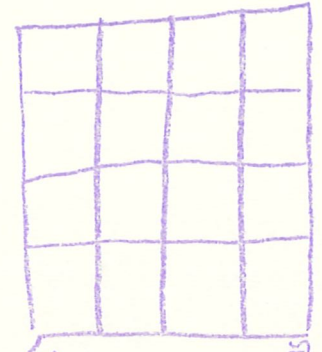
- A Reflexive
- B. Symmetric
- C. Antisymmetric
- D Transitive

7. Show $f(x, y, z) = x' + yz'$ is functionally complete

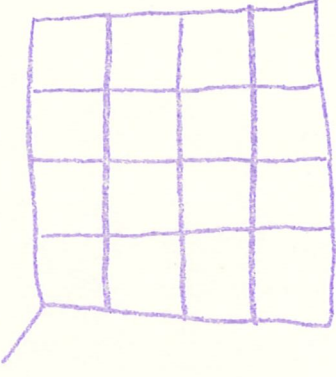
8. Give a state diagram which recognizes the sequence 001, 0001, 00001, ...
Clearly label your starting state
two or more zero's

9. For $f(w, x, y, z) = \sum(0, 2, 4, 6, 7, 10) + \sum\phi(3, 5, 8, 15)$

AB Find all minimal sum of products expressions for f



CD Find all minimal product of sums expressions for f



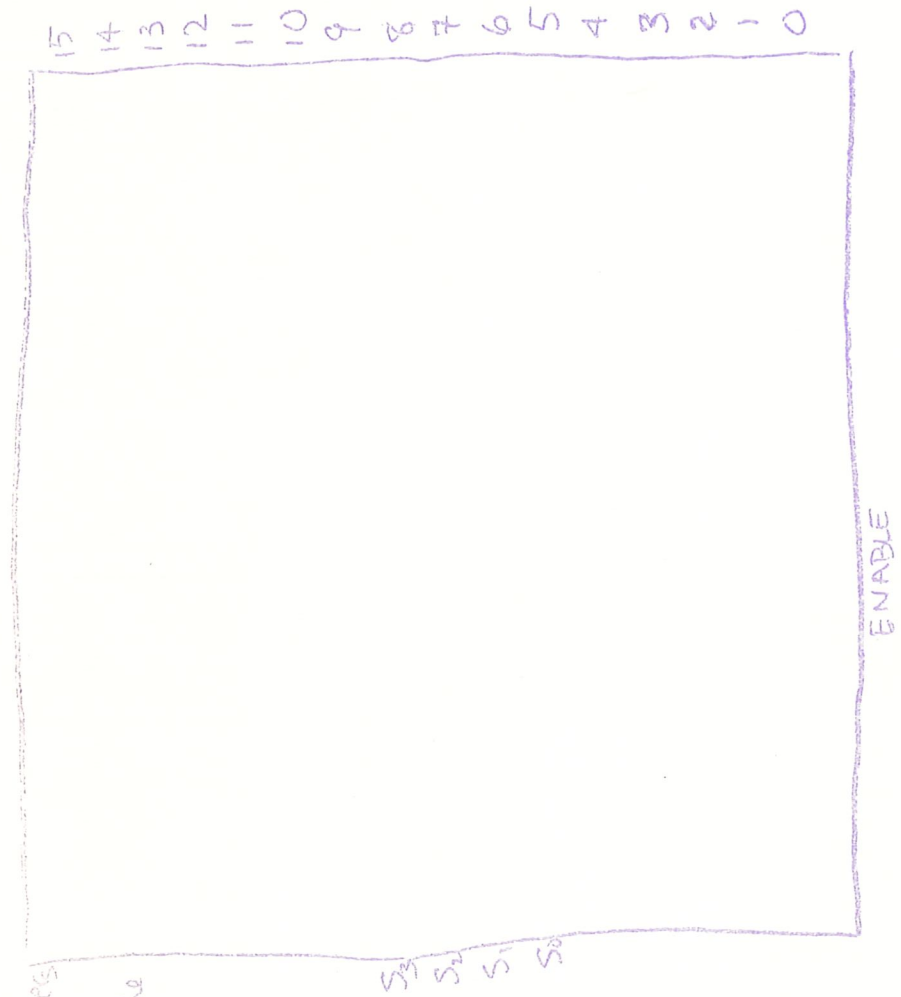
E. Which are minimal overall?

10. Define or state what it means

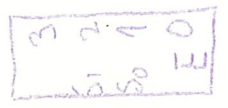
A. Symmetric function $f(x, y, z)$

B. Irreflexive relation R on X

C. the sup of x & y



11. Use 5 2x4 decoders with enable (like one below) inside the box to realize the 4x16 decoder shown

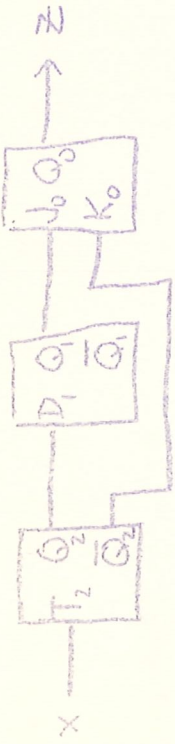


12. Complete the timing diagram below. All gates have 4 ns delay. ARROWS are required

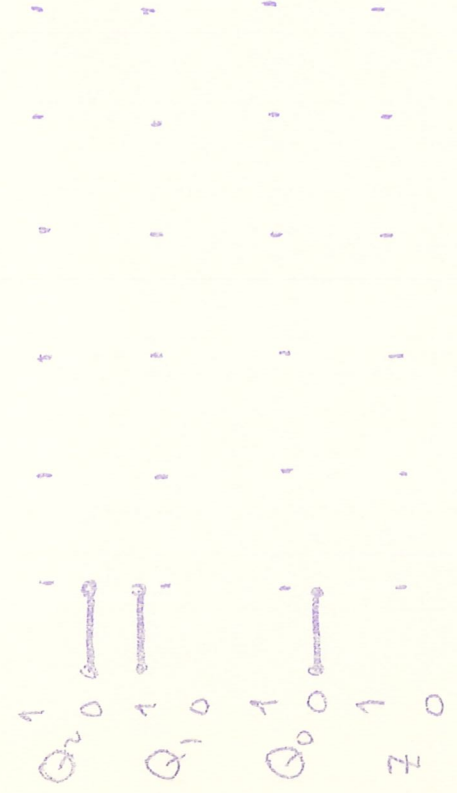


time

13. A) Fill in the state table to right for the circuit below



B Complete the following assuming the input x is always 1



Next State / Output	X=0	X=1
$Q_2 Q_1 Q_0$	000	
	001	
	010	
	011	
	100	
	101	
	110	
	111	

14 Realize the state table below using two JK flip flops and as few gates as possible.

$Q_1 Q_0$	X=0	X=1
00	11/0	10/0
01	01/0	10/0
11	10/1	00/1
10	11/0	00/0

Note Gray code order

15. Prove or Disprove. (For Any Boolean Algebra)

A. $xy + x'z = [(x+y')(x+z')(yz)']'$

B. $x'y + xz + x'z = yz + x'z + y'z + x'y'z' + x'y + xy'z'$

16. Prove by INDUCTION: No matter which state you start in, after the input sequence for $n \geq 0$

1101 0001 0001 ... 0001

$\underbrace{\hspace{10em}}_{n \text{ repetitions}}$

the current output is 1 and the next state is C

	x=0	x=1
A	D/0	A/0
B	A/0	A/0
C	B/0	A/0
D	D/0	C/1