COT 3132 Digital Networks The good doctor Bellenot

off 211 Love
off hrs MWF { 12:30 – 1:00
2:15 – 3:00

TEXT: Kohavi 2nd Ed "Switching & finite automata theory"

GRADES: The classic 90, 80, 70, 60 cut offs

based on
1 Final	30%	
3 Tests	45%	(15% each)
weekly TP's	15%	(See TP sheet)
daily homework	10%	

ATTENDANCE is required. Six absences is an automatic fail. A student who does not turn in homework at the beginning of class is considered absent.

HOMEWORK: Only some homework problems are graded. Usually it is all right or all wrong (i.e. no partial credit)

TESTS: In class closed book and closed notes. There will be proofs on the tests.

MATERIAL CHAPT's 1, 2, 3, 4, 5, 6, 7, 9, 16 and Section 8.1

TEST PROBLEMS (better known as TP's)

[Note this sheet does not apply to HW.]

1. RULES

A. They must be on 8½ by 11 paper.

B. They must be written in ink.

C. They must use only one side of each page.

D. If there is more than one page, then the pages must be stapled or paper-clipped together.

Failure to follow any rule costs a point each.

2. Grades

A. Graded on a 0 to 10 basis.

B. Graded on your reasoning, your ability to express your reasoning, neatness and your English.

3. Your TP average is computed using only your best n out of the m assigned where $\frac{n}{m}$ is roughly $\frac{2}{3}$.

4. Since TP's are assigned a week in advance of their due date, the solutions handed in are assumed to be carefully worked out. In ANY CASE they will be graded as if they were.

5. They must be your OWN work.

TP2 Digital due Wed 14 Sept 83

Define the binary operation | (Nand or Sheffer stroke) on any Boolean Algebra by

$$x|y = (xy)'$$

A. (2 points) Show $x|(y|z) \neq (x|y)|z$

B. (2 points) Show $x|x' = 1$ and $x|1 = x'$

C. (6 points) Define $f_0(x) = x$ and for $n \geq 0$ define $f_{n+1}(x) = x|f_n(x)$

Show by induction that for $n \geq 1$

$$f_n(x) = \begin{cases} x' & \text{if } n \text{ is odd} \\ 1 & \text{if } n \text{ is even} \end{cases}$$

TP1 induction $a_n = (a_{n-1})^2 \Rightarrow a_n = 2^{2^n}$ $a_0 = 2$

TP3 realize $x', x+y, x \cdot y, x \oplus y, xy + x'y'$ by NANDS ALONE & NORS ALONE } few gates as possible

TP 3 due Mon 19 Sept 83 Digital

The basic circuit of TTL (Transistor-Transistor Logic) is the NAND gate (which can have more than two inputs.)

The basic circuit of ECL (Emitter-Coupled Logic) is the NOR gate.

In each case, you need ~~not~~ no other gates since all other gates can be obtained from NAND gates alone or NOR gates alone. {This ~~is~~ property is called functionally complete}.

Your problem is to construct circuits that realize the given function (switching function) using NAND gates alone and then using NOR gates alone. Only unprime inputs x, y, z are available. Your answer should use as few gates as possible. You may use gates with more than two inputs

A. $f(x) = x'$ B. $f(x,y) = x+y$ C. $f(x,y) = xy$

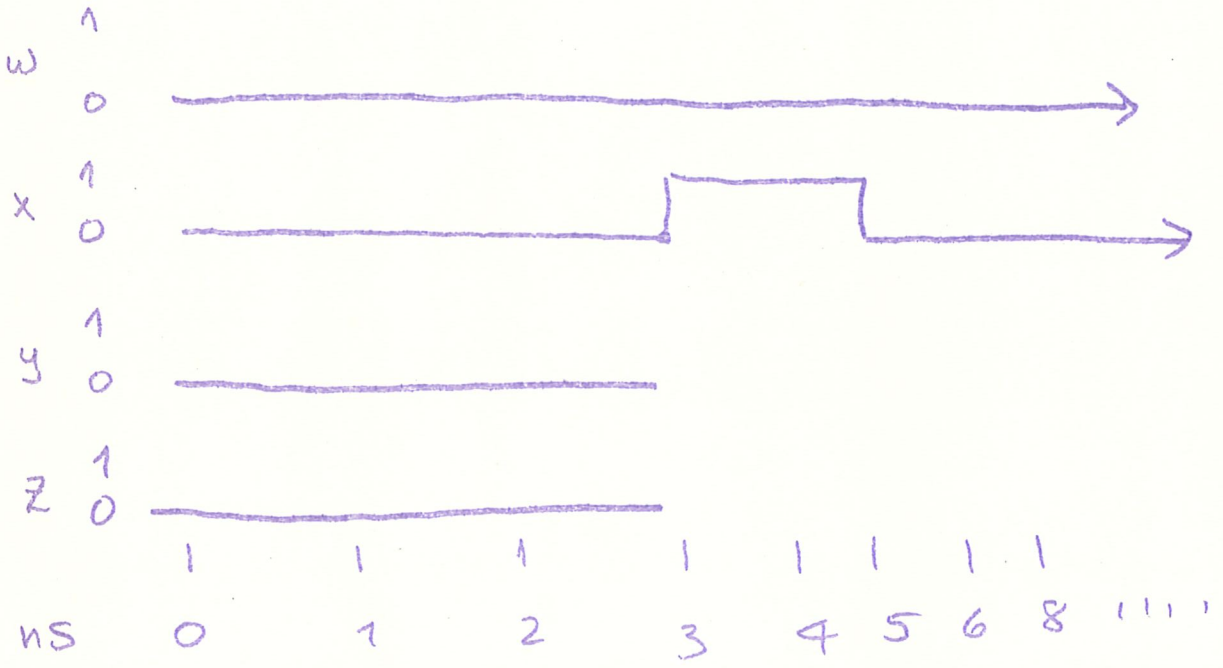
D. $f(x) = (xy)'$ E. $f(x,y) = (x+y)'$ F. $f(x,y) = x \oplus y$

G. $f(x) = x \oplus y \oplus z$ H. $f(x,y,z) = xy + yz + xz$

(Note G & H worth twice A, B, C, D, E and F (ie 2 pts ea vs 1)

Make your circuits NEAT

TP4 due Wed 28 sept 83 digital



Complete the timing diagram if all gates

A. Have a delay of zero n.s.

B Have a delay of one n.s

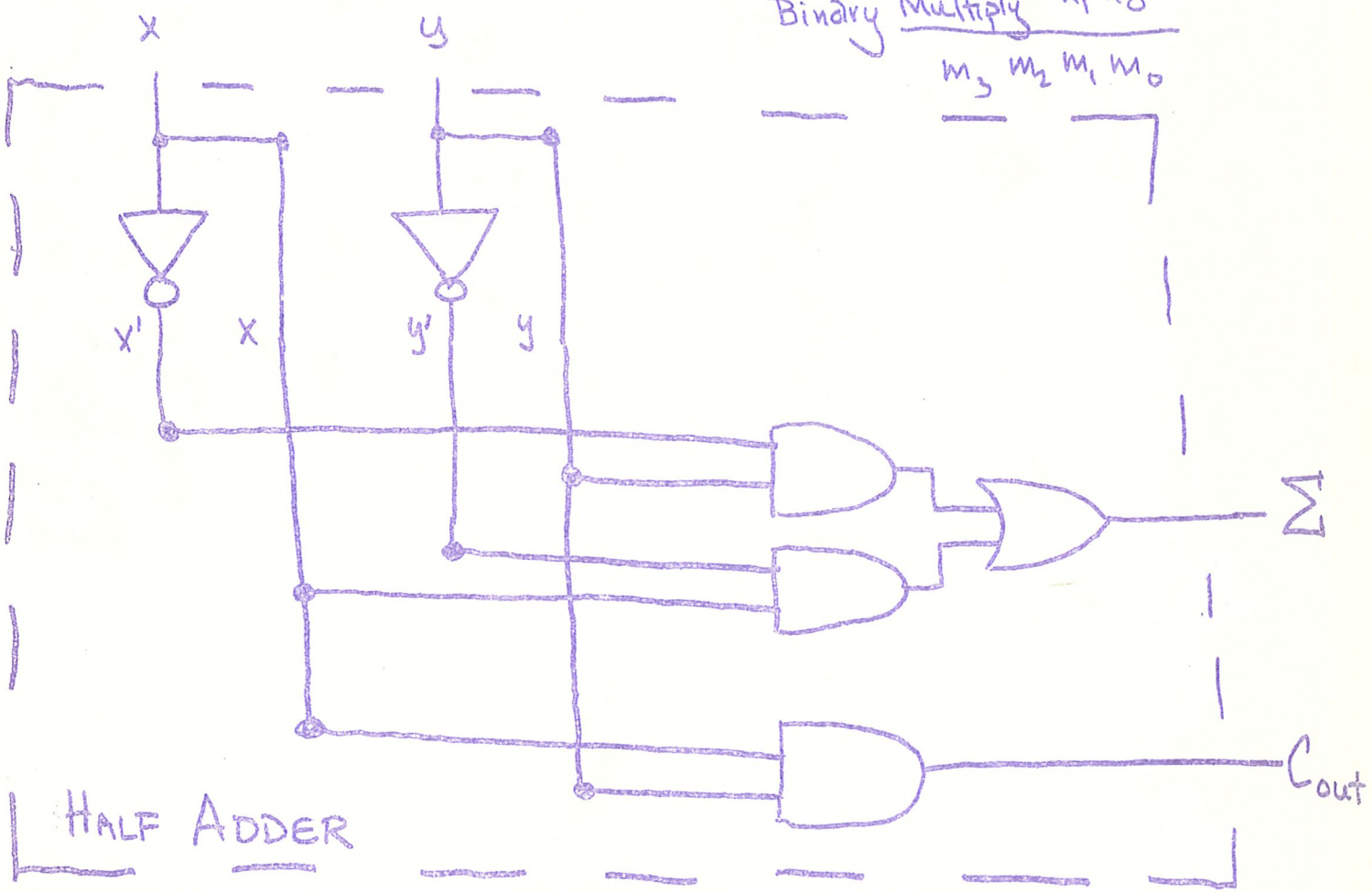
C. Have a delay of two n.s

D. Have a delay of three n.s.

TP 5 due Mon 10 Oct 83 digital

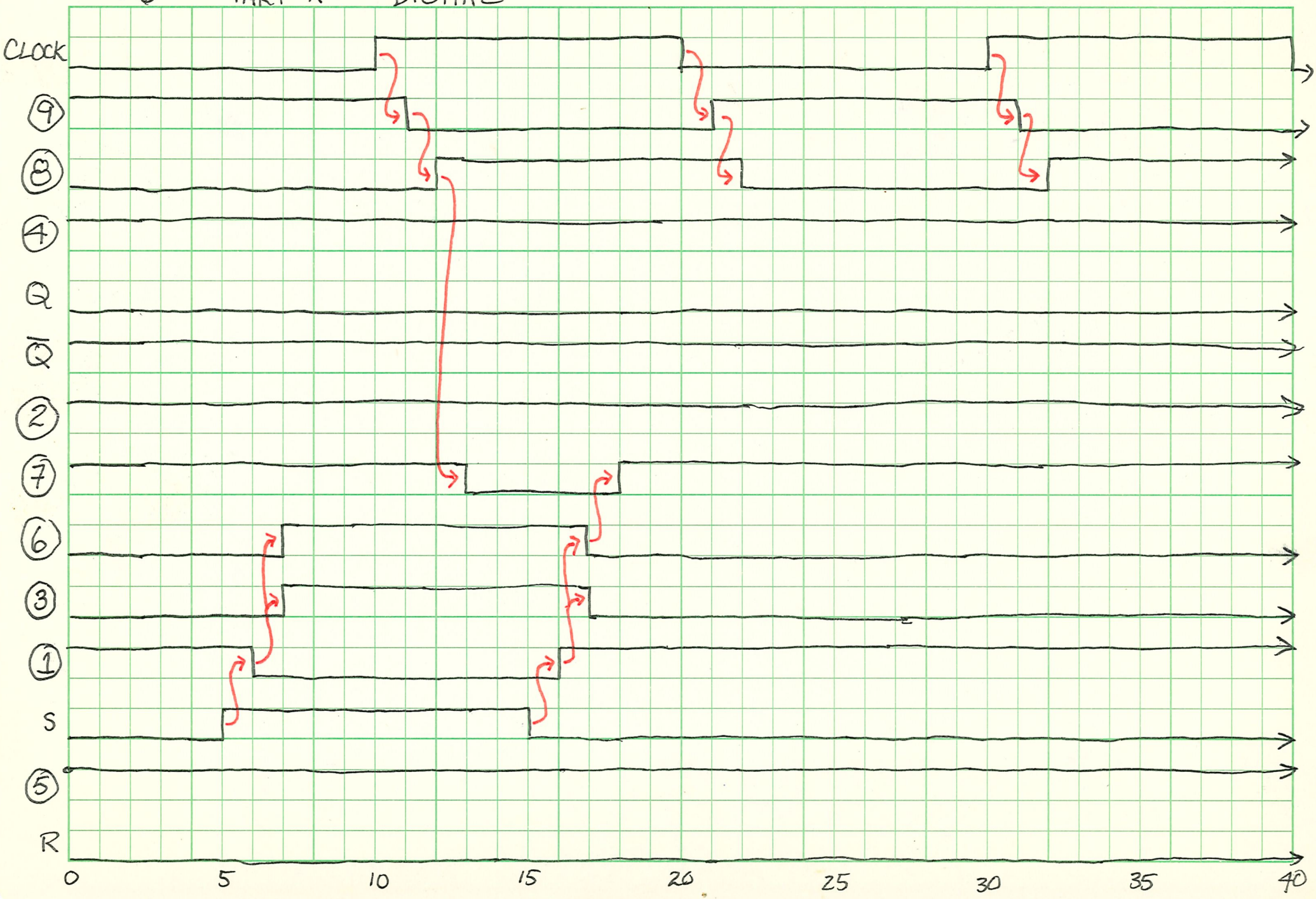
Design and realize a 2-bit binary multiplication unit. (Your circuit ~~shall~~ is to meet the standards below like the half-adder shown.) I.E. you have 4 inputs x_1 x_0 y_1 & y_0 and 4 outputs m_3 m_2 m_1 & m_0 so that

$$\begin{array}{r} y_1\,y_0 \\ \text{Binary Multiply} \quad x_1\,x_0 \\ \hline m_3\;m_2\;m_1\;m_0 \end{array}$$



1. EACH OUTPUT IN MINIMAL SUM OF PRODUCTS
2. ALL LINES HORIZONTAL OR VERTICAL
3. NO "JUMPS" OR "HOOPS"
4. INPUTS AVAILIABLE ONLY "ONCE" AND ONLY UNPRIMED

TP6 PART A DIGITAL



4 Squares to the Inch

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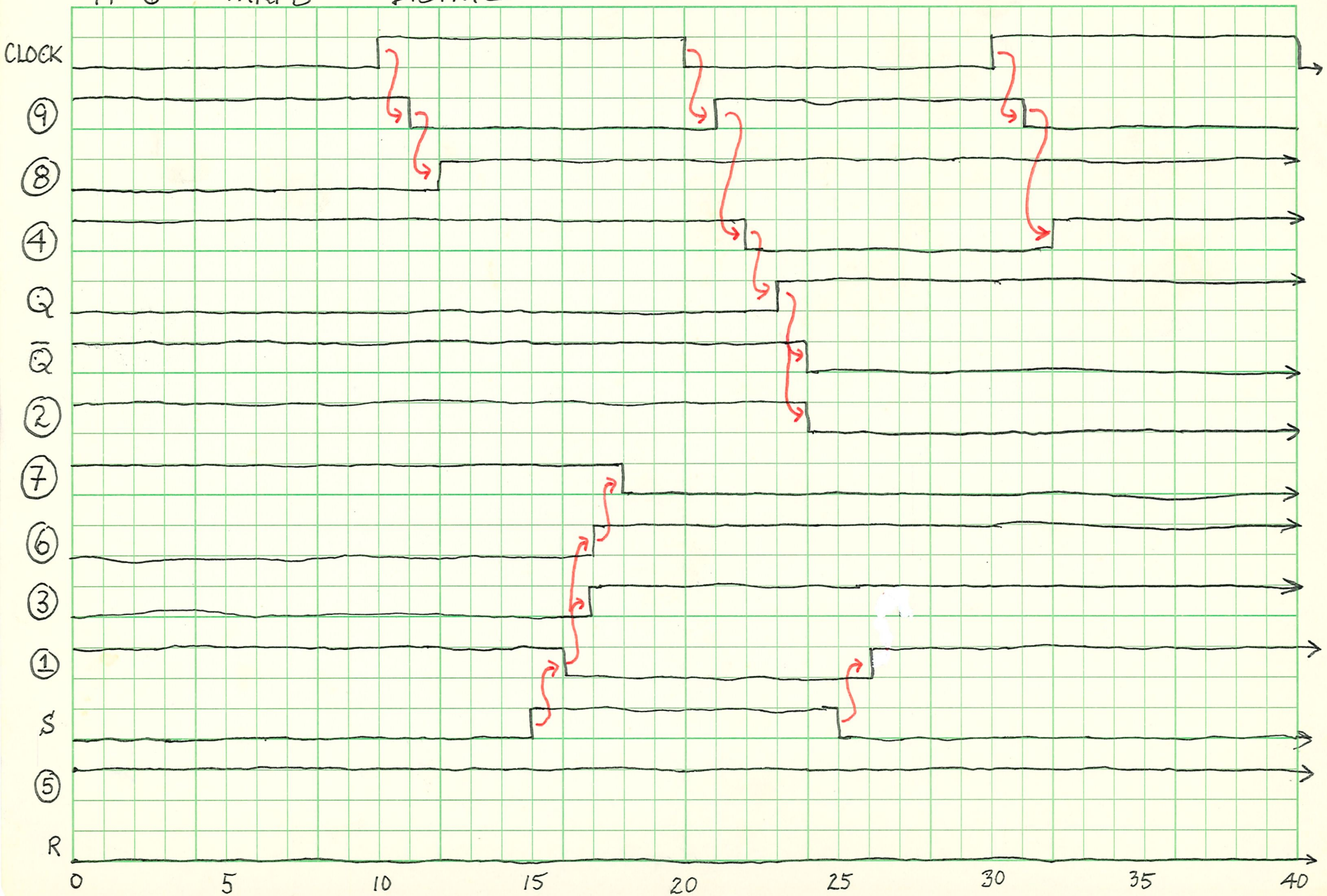
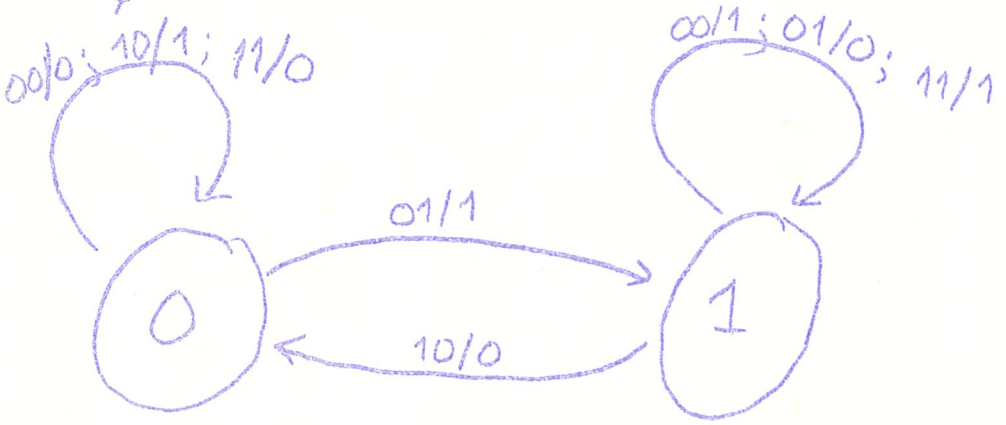
TP 6 PART B DIGITAL



TP 7 due Mon 24 OCT 83 digital.

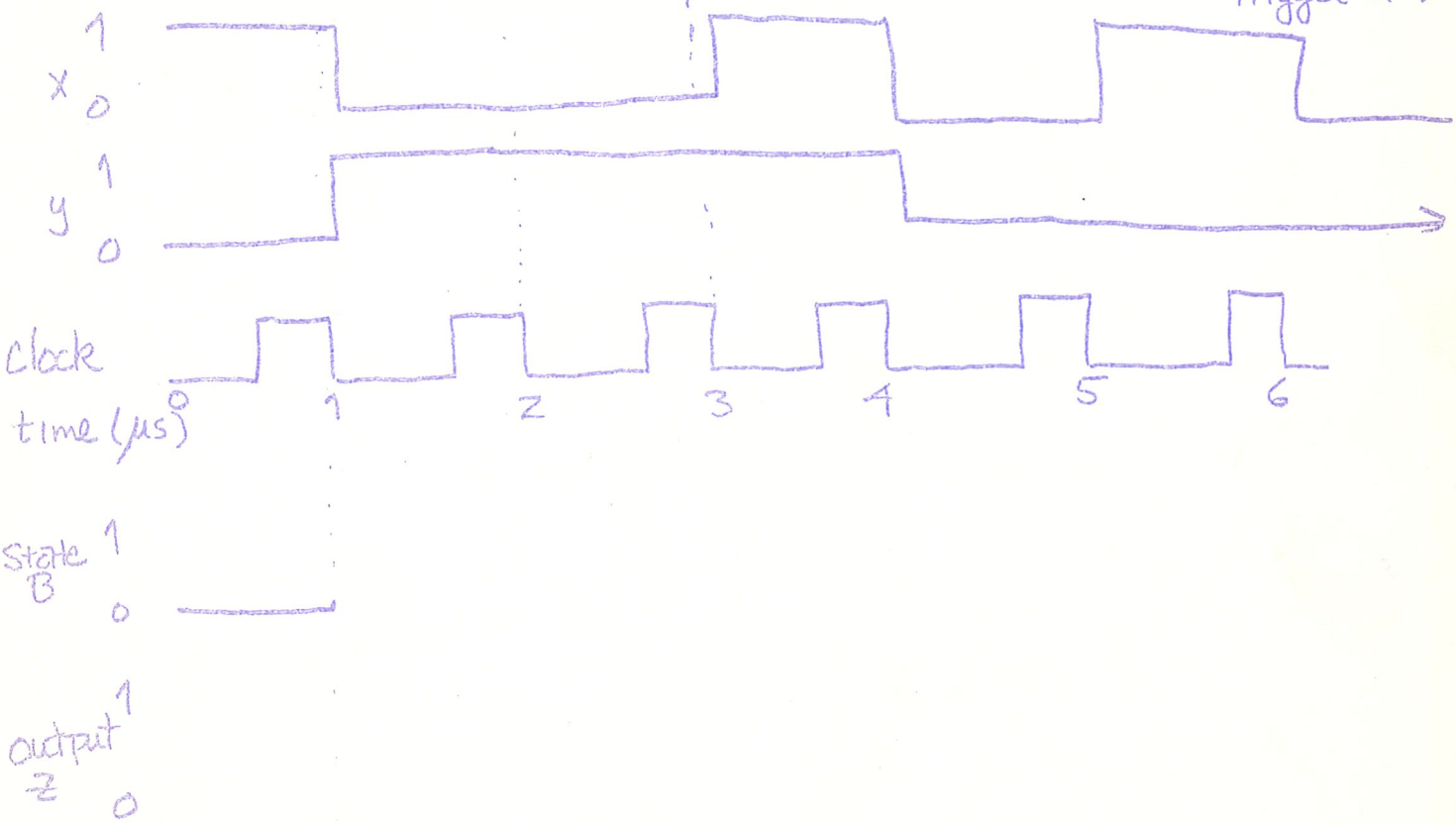
Use a T flip-flop to realize the following state diagram

(inputs xy/z output)



B is state variable

and complete the following diagram (T is neg. edge triggered)

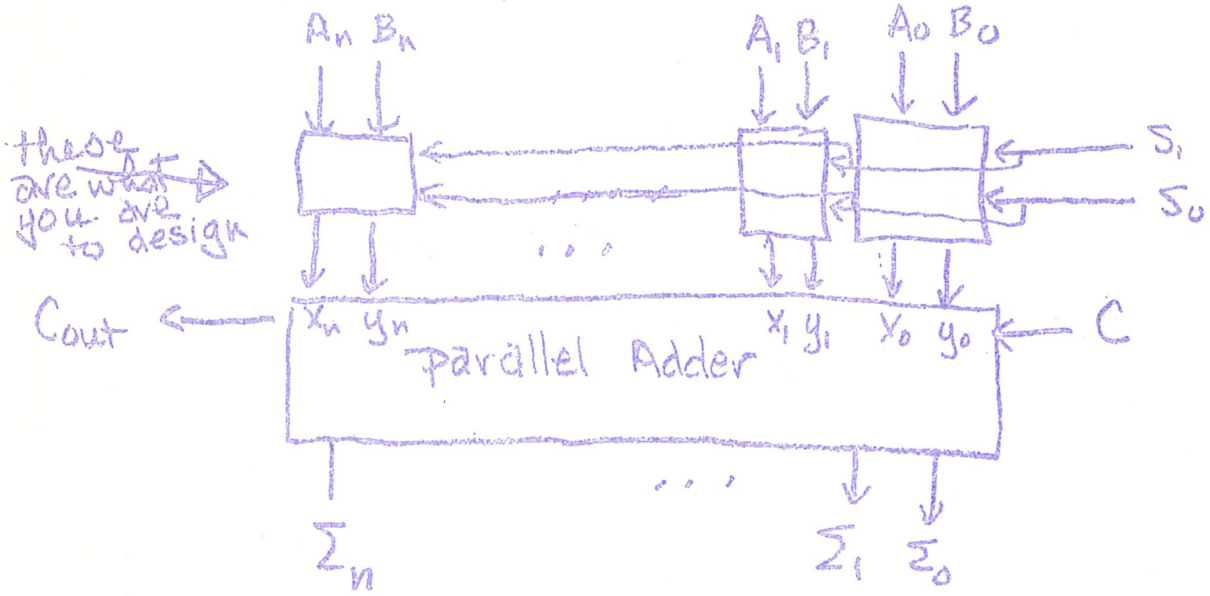


TP 8 due Mon 31 Oct 83 digital

An Arithmetic circuit has two "selection variables" or "controls" S_1 & S_0 together with C [carry in] so that

S_1	S_0	C = 0	C = 1
0	0	A + B	A + B + 1
0	1	A	A + 1
1	0	$\bar{B}$	$\bar{B}$ + 1
1	1	A + $\bar{B}$	A + $\bar{B}$ + 1

(Here $\bar{B} = B'$) (And + is addition)

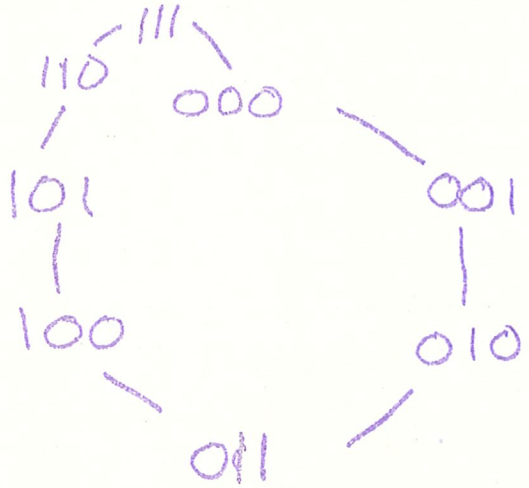


Determine the circuit (and draw it) that must be incorporated will a full adder in each stage of the arithematic unit to produced the desired outputs above.

TP 10 due Wed 16 Nov 83 digital

Design and realize a 3-bit counting register X made from three T-flip-flops with controls E (enable), L (load), C (count), U/$\bar{D}$ (if 1 going up, if 0 goind down. It has three inputs $I_2 I_1 I_0$

E	L	C	U/$\bar{D}$	Current State $X_2 X_1 X_0$	Next state
0	ϕ	ϕ	ϕ	$Q_2 Q_1 Q_0$	$Q_2 Q_1 Q_0$
1	0	0	ϕ	$Q_2 Q_1 Q_0$	$Q_2 Q_1 Q_0$
1	1	ϕ	ϕ	$Q_2 Q_1 Q_0$	$I_2 I_1 I_0$
1	0	1	1	$Q_2 Q_1 Q_0$	$R_2 R_1 R_0$ (clockwise)
1	0	1	0	$Q_2 Q_1 Q_0$	$S_2 S_1 S_0$ (counterclockwise)



↻ direction counting up

↺ direction counting down

TP 11 due Wed 23 Nov 83 digital

Use an RS flip-flop to design a DE-unit

DE	current	next		
ø ø	Q	Q	← E=0	HOLD
y 1	Q	y	← E=1	LOAD

and use three of them to realize the shift register below

$C_2C_1C_0$	CURRENT	NEXT	
0 0 0	$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	HOLD
0 0 1	$Q_2Q_1Q_0$	$I_2I_1I_0$	LOAD (I_j inputs)
0 1 0	$Q_2Q_1Q_0$	$Q_1Q_0I_0$	SHFT LFT W/ LOAD
0 1 1	$Q_2Q_1Q_0$	$Q_0Q_1Q_2$	REVERSE
1 0 0	$Q_2Q_1Q_0$	$Q_2Q_2Q_1$	ARITH SHFT RT
1 0 1	$Q_2Q_1Q_0$	$Q_0Q_2Q_1$	ROTATE RT
1 1 0	$Q_2Q_1Q_0$	$0\,Q_2Q_1$	SHFT RT W/ZERO FILL
1 1 1	$Q_2Q_1Q_0$	$Q_2Q_0I_0$	ARITH SHFT LFT W/LOAD

USE A 3x8 DECODER W INPUTS $C_2C_1C_0$ TO GET "CONTROL LINES"

TP 12 Use 5 4x2 priority encoders to make 16x4.