ORG Test 2 4 MAR 85 (Post increment into breaks) by _____

Show ALL work 1-4 worth 10 pts each 5-8 worth 15 pts each

1. AB. It has been decided to replace a μ-memory of 1024 words each 100 bits wide with a μ-memory/nanomemory combination. If there are only 128 different bit patterns in the old μ-memory how many bits would be saved with the nanomemory?

8. Carefully "step by step" illustrate the restore method when

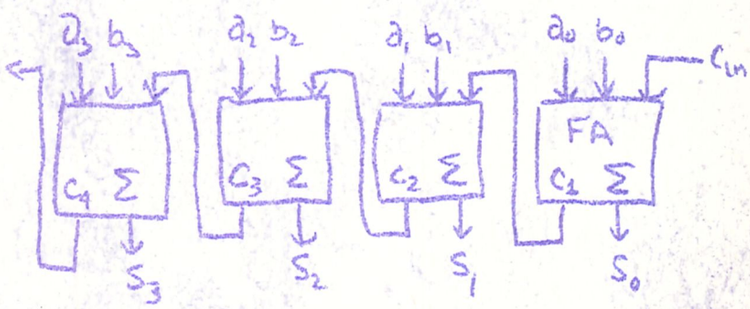
C. Fill in the blanks with H (Horizontal) V (Vertical) B (Both) N (Neither)

7. New μ-memory is _____ nanomemory is _____

2. AB Formulate a mapping process from (macro) op-codes to (μ) control memory addresses given that μ-memory has 1024 words, op-codes are 5-bits wide and 8 control words are needed for each macro-op.

C. Illustrate your map with the op-code 13_{10} give the address in binary!

3. For the 4-bit parallel adder to right, write down the boolean expression which will yield the following flags

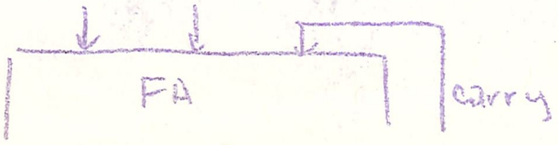


A. C= B. S= C. Z= D. V= E. FE=

4. For the function table to right draw the circuit of a typical stage of the arithmetic circuit.

$S_1 S_0$	$C_{in}=0$	$C_{in}=1$
00	A+B	A+B+1
01	A-1	A
10	B-1	$\overline{B}$
11	B	B+1

A_i B_i



5. Write μ-code in the Chapt 8 style which does XCHG: AC ← M, M ← AC. To start you off right, worry about effective addresses. The op-code is 7.

6. A 12-bit SP (stack pointer) has been added to the chapt 5 computer. SP points to TOS (top of stack) and grows toward low memory. Your task is to write the execution cycles (with controls) for CALL (op code r) and RETURN (op code s)

A. CALL

B. RETURN

7. The Prob 7 computer is a 16-bit machine with 4 general purpose registers and zillions of addressing modes. Opcodes are 16-bits wide and instructions which need an address or constant are two words long. The second word is the address or constant.

Registers	
Name	Contents
R0	13
R1	4
R2	5
R3	8

PC = 0 and the contents of the machine are given to the right. The op code I is for the instruction which loads register R0. Give the contents of R0 after this instruction is executed, if the source is in the addressing mode.

Memory Address	Contents
0	I
1	3
2	10
3	6
4	1
5	2
6	7
7	12
8	9
9	0

A. Immediate ___ B. Direct. ___ C indirect ___

D. Register R1 indirect ___ E. Relative ___

F. Indexed by R2 ___ G. Register R3 ___

H. Relative with index R1 and displacement ___

8. This problem is on the 68000 (by Motorola)

A. Register width _____

B Address bus width _____

C. Word size _____

D. Each memory address contains how many bits ____

E. In terms of instruction formats it's a _____ address machine.

F. Which addressing mode is missing ____

G. Auto-increment is ____ increment

H. Auto-decrement is ____ decrement

I. How many Mega Bytes can the 68000 directly address ____

Addressing Modes

JK In the relative mode, the displacement is a word long what is the memory range of this mode

L. In relative with index and displacement, again the ~~source and~~ computed address and the address bus are not the same size. What is done?

Immediate

Instructions are one word + extentsion (for data or address as needed) Give the length in bits for each of the following

M. Quick Immediate ____ N. Immediate-word ____

O. Immediate long word _____

PQ The immediate-word is shorter than its destination what is the range of integers

RST. Why is their a quick immediate mode?
(what is the trade off and why is it worth while?)

rev/sec = 81.68... in/sec 6.8... ft/sec
408 ft/min
25504.423 ft/hr 5 mi/hr

15&16 Designing a digital bicycle speedometer. The idea is to count revolutions of the front wheel (in rev/sec) and translate this into speed (in mph). The equation $r = 13s$ is helpful, where r = number of revolutions of front wheel per second and s = speed in miles per hour. 775.69 rev per mile

mph miles/hour hour/min min/sec ft/mile in/ft 1 rev/in

A. Assume the register AR contains the number of revolutions in the last second. If speeds of at least 100 mph need to be accurately read, how wide must AR be? 11

$s = 100$ $r = 1300$

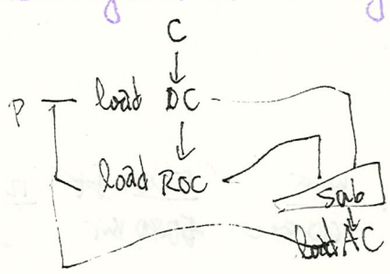
BC. Assume the register C contains the total number of revolutions since the speedometer was last turned on. If distances of at least 1000 miles need to be accurately reported, how wide must C be? 24

$r_{/sec} = 1000/hr$ 3600 hr/sec 3,600,000 2^{24}

D. To get the correct value in AR from the value in C we add registers OC (old C) and ROC (Real Old C) the same width as AR. Assume the control line p is "1" for exactly 1 clock cycle per second, then the micro-op P: ROC ← OC, OC ← C (the correct number of low order bits) is ~~done~~ added to the system. Explain how the value for AR can be obtained.

AR = OC − ROC

EFG Draw a block diagram of the system so far (when do you load AR?)



HI A "look up" table is used to translate the value in AR to the correct output codes to display the current speed. The output display has 3 digits (like 37.2) and each digit is displayed by a 7-segment display unit (decimal point is always on) what size (ie $2^n \times m$) ROM is needed? $2^{11} \times 21$

JK. We are almost done with output, but the display units use too much of the battery an so we need a control line q which is "1" for exactly 1 clock cycle some where between 50 and 100 times a second. The clock rate is 1 Mega Hz and we add another register D with μ-op 1: D ← D+1 and let q be the boolean value of (D=0). Find the width of D 14
(Values somehow will only be displayed when D=1, saving lots of current (i.e. battery juice))

10,000

$50 < \frac{10^6}{2^n} < 100$ $\frac{1}{2}2^n < 10^4 < 2^n$

n = 14

LMN Finally we start on input. A tiny magnet is put on one spoke of the front wheel and a magnetic sensor is placed on the front fork. Spinning the front wheel, we find that the sensor "feels" the magnetic field for 1/32 of every rotation of the wheel. The clock rate is 1 MHz, how many clock pulses does the sensor "feel" the magnetic field each revolution if the bike is going 100 mph? 24.03 if the bike is going 1 mph? 2403.84 cm

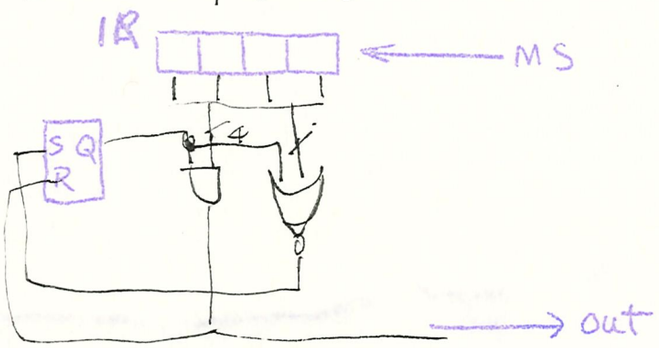
$r = 1300 \frac{rev}{sec}$ $10^6 \frac{clk}{sec}$ $\frac{10^6}{1300}$ cl/rev $\frac{rev}{32 \cdot \frac{1}{32} rev}$

OP If the sensor sends "logic 1" to the speedometer when it "feels" the magnetic field and "logic 0" otherwise, This input is serially loaded into the register IR which is four bits wide. label the sensor output line MS (magnetic sensor) write the μ-op which does this and include "control" part in the μ-op.

1: shl IR, $IR_0 \leftarrow$ ms

QRSTUVWXY:

Draw a circuit which translates the "leading edge" of MS into a 1 clock pulse long output (i.e. so that out: C ← C+1 keeps the correct count of the number of revolutions) once Q=1 & IR=1111



Note that ms ⎍ clock ⎍ out ⎍ until the next leading edge

OUT is "1" for one clock cycle then Out is zero

Za: There are 2 states (Q=0) and (Q=1) describe what each is looking for

(Q=0): clear

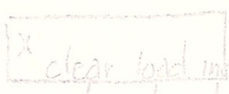
(Q=1): hunt

b: Now we are ready to initialize the speedometer, which of our registers need to be initialized (AR, C, OC, ROC, D, IR) if we don't care if it gives incorrect speeds or distances for 30 secs or so but it needs to be correct after 1 min of operation.

C

cd How would you initialize the value of C? C ← 0

1. The register X, (with clear, load, increment) is effected by the μ-op's C_0t_0 : X ← X+1 ; C_3t_1 : X ← PC ; $q_7C_2t_3$: X ← 0 ; $q_5C_2t_1$ X ← MBR(AD) ; C_0t_0 X ← MAR ; Draw the gates & control lines need to "control" X.



2. Describe in detail what is going on in the I/O system of Ch 5 computer when A. FGI changes from zero to one B. FGI changes from one to zero C. FGO changes from zero to one D. FGO changes from one to zero. E. Transfer to and from INPR and OUTR are possible from what places in the Ch 5 computer system?

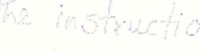
3. Write down μ-op's which when done "in sequence" will move the memory word pointed to by the address part of the memory word in $(0A7)_H$ to the memory word in $(3BB)_H$

4. Interrupts on the Ch 5 Computer, A. The interrupt vector is? B. What is stored at the interrupt vector? C. Can an interrupt be interrupted? (yes/no) Why? D. What is the next to last instruction of the interrupt routine and what does it do? E what is the last instruction of the interrupt routine and what does it do.

5. Using $2^{10} \sim 10^3$, 80 char/line, 40 line/page, 400 page/book estimate the following A. A mainframe harddisc holds 512 Mega Char, how many books? B. A Tape 2560 ft inches long holds 1600 char/inch, how many books? C. A SSSD 8" floppy disk has 77 tracks (say 80) of 26 sectors (say 32) of 128 char, how many pages.

6. Add two new registers (12 bit) FRONT & REAR to the ch. 5 computer. These are pointers to a memory queue. Write the execution cycles for two new instructions. A Enqueue (op code r) puts the contents of AC to where REAR points and decreases ~~front~~ rear. B. Dequeue put the memory contents at where FRONT points in AC and decreases front. Include control and timing in the μ-ops.

7. Implement (ie draw circuit) of a 5-bit register (using T flip-flops) which has Two's COMPLEMENT control line Z.

8. If the μ-ops to the right are done in sequence
   A. If $M(123_H)$ contents is $7F\emptyset A_H$ before this sequence, what is its contents afterwards?
   B. What does the sequence of μ-ops do?
   C. Obviously this sequence doesn't fit into our 4 cycle execution state, however it is possible to write a sequence of μ-ops in the Ch 5 execution state style which on the instruction  does the same operation to M(m). Do so including control and timing.

$MAR \leftarrow 123_H$
$MBR \leftarrow M$
$AC \leftarrow MBR$
$AC(1\text{-}8)_{Top} \leftarrow AC(9\text{-}16)_{Bot}$, $AC(15)_{Bot} \leftarrow AC$
$MBR \leftarrow AC$
$M \leftarrow MBR$

9. Write −12 in an 5-bit register using A sign-magnitude B 1's complement C. 2's complement D. Excess 16 notation (bias exp)

10. Explain in detail how subroutine calls are made in the ch 5 computer Subroutine returns. Is recursion allowed? Can A call B call C call A? Can A call B call C call D?

11. A computer has 128K of 29 bit words of memory. Machine instructions fit into one word with an address field, a register field, an indirect bit. There are 32 registers R0 – R31. A. How many such op codes are there. B what is the width of the PC? C MAR? D. MBR? E R0–R31? (most likely) F (second most likely?). Draw a reasonable instruction format with the number of bits in each field.

12. A Rewrite q'r: if (I=0) then PC ← PC+1 without the if then if I is 4-bits wide. B. Rewrite q'r: AC ← $\overline{AC}$ + 1 without the q' in the control. C. If the micro-op abc: A ← B, B ← C, C ← A can happen in a computer then the computer must have how many internal buses?

13. Write a sequence of machine instructions for the Ch.5 computer which will. A. AC ← M[m] V M[n] m, n locations in memory B. AC ← M[m] − M[n] C. PC ← M[m](Address) D. Suppose the AC contains an instruction say I, write a sequence of instructions which will eventually execute this instruction.

14. A study of programs on the ch5 computer shows that 60% of the executed instructions are either register ref or I/O instructions and 40% of the others are indirect. And the average time of program execution is T. The same program mix is run on the Jazzed up version where I/O & reg ref instructions are executed in c_0t_3. What is the average program time on the the JAZZY Ch5 computer.

15. Implement t: AC ← card(AC) where AC is a 4-bit register and Card(AC) is the number of 1's in the AC. Use your favorite flip-flops, a decoder and an encoder.

16. Draw an analogy between interupts and phone calls. A. What acts like ION, IOF? B. What is the alternative to interupt driven phone calls. C. What feature does the Ch5 computer have that the absent minded professor have in regards to this issue.

17. A Machine instruction NOP (no operation) is not do nothing at the μ-op level. In the ch 5. computer which registers must change? which registers can change? (time period start of fetch of NOP to start of fetch of next instruction.)

18. Like 6 only with SP (stack pointer) register and the operations are push and pop. See Also Prob 5-13

19. In Ch5 computer add A (1 bit flag) initially cleared; T1, T2 12-bit registers, NU 4-bit register. Change q_3 so that the μ-op to left are used. Note the change in state transistion from execute.

What does it do? Why would you want to?

$A'q_3c_2t_0$: T1 ← MBR(AD), MAR ← PC
" t_1: MBR ← M, PC ← PC+1
" t_2: T2 ← MBR(AD), NU ← MBR(1-4)
" t_3: A ← 1, stay in c_2
$Aq_3c_2t_0$: MAR ← T1, T1 ← T1+1
" t_1: MBR ← M, MAR ← T2, T2 ← T2+1, NU ← NU−1
" t_2: M ← MBR
" t_3: if(NU=0) then A ← 0 & goto fetch else stay in execute

ORG TEST 1 spring('85 NAME _____

Problems 1-4 worth 10 points each, 5-8 worth 15 points each.
Show your work, Be neat, and Good luck.

1. Complete the table to the right for the Chapt. 5 computer.

Register	Full Name	Width
PC		
AC		
MAR		
OUTR		
MBR		

2. Using an 8-bit register write in the following "codes": A. -35 in signed-magnitude _____

B. -35 in 1's complement _____ C. -35 in 2's complement _____

D 52 in BCD _____ E. '3' in ASCII with the most significant bit ODD parity (given '0' is decimal 48) _____

3. Write a sequence (program) for the Chapter 5 computer (i.e. Machine instructions) which will "do" the Pascal code to the right. X and Y are locations in memory containing the values of X & Y. The value Z is ~~not~~ nowhere in memory.

```
While X ≠ 00 do
  begin
    Y := Y+2;
    X := X+1;
  end;
Y := 0
```

4. The super-Jazzy Chapt 5 computer has all states 3 cycles long and both register reference and I/O instructions are executed during the last fetch cycle (cot$_2$ now). The program mix of executed instructions is 1% interupts, 40% register reference or I/O instructions, 29% direct memory reference and 30% memory indirect instructions. The average time of a program on the old Chapter 5 computer was T. If the same program mix is run on the super-Jazzy computer what would the average program time be?

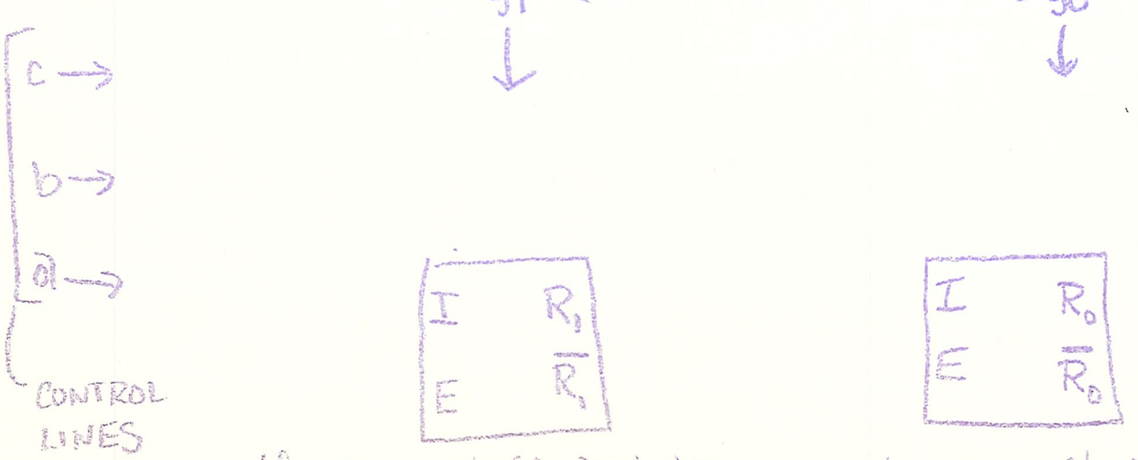
5. Using the execution cycle of the Chapt. 5 computer (4 clock cycles) write down the necessary controls and μ-ops which will do the following operations (machine instructions) with the given op-code. Assume a chapt 5 fetch and that ⊕ is available.

A. M ← AC, AC ← M op-code "r" B. M ← M⊕AC (AC doesn't change) op-code "s"

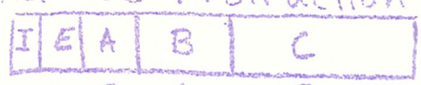
6. Write down μ-ops for Chapt 5 computer which when done "in sequence" will swap the contents of the memory word pointed to by the address potion of $M[123_H]$ with the contents of the memory word pointed to by the address portion of $M[ABC_H]$. This can be done in 12 cycles, using more will cost points.

7. A. A IE flip-flop has 2 inputs I & E. When E=1 then the contents of I is loaded. When E=0, the flip-flop is in a hold. (i.e. E = enable I = input). Construct an IE - flip-flop using a JK flip-flop, (and some gates)

BC. (worth 10 pts, A worth 5) Construct a 2-bit register R with IE flip-flops which does a: R ← 0; b: R ← y, c: R ← $\bar{y}$ where y are the two input lines



use the given stuff and assume abc = 0 always

8. A GRAND new design for the chapter 5 computer is being considered. First a new 12-bit register X is added (X for indeX). Second the instruction format is changed. The fields are 

with the widths below.

If E = 1 then we have a full address ~~memory word~~ reference that is I = indirect bit as before, A is the op code, and B & C together give the memory address

If E = ~~4~~ 0 ~~then~~ and A & B ≠ 0 then we have an indexed memory refrence, that is I = indirect bit ~~as before~~ and if I = 0 then the effective address is X + C or C is the offset from the contents of X to find the effective address. If I = 1, this is done twice. ~~as before~~.

If E = 0, A = 0 & B = 0 then I = 0 says it is a register reference instruction and I = 1 says it is an I/O instruction ~~de~~ both determined by the field C.

Another parallel adder is added to the CPU.

A. What is the maximum number of
   1. full address instructions?
   2. indexed memory reference instructions?
   3. register reference instructions?

B. The instrudion is 00 000001 11100011 is an ADD to AC write the execution cycle of this instruction. Call the op-code P_1, you have four clock cycles. (Assume Ch 5 fetch)

C. Write the indirect cycle (ICP) for this system, Assume a chapter 5 fetch with all contents of MBR saved in registers I, E, A, B, C like I & OP are done in Ch 5

D. What is the main advantage of this design over that of Ch 5. And what is the main disadvantage?

[illegible]

2. Describe in [illegible] what [illegible] when A. [illegible] changes [illegible] B. [illegible] C. [illegible] changes [illegible] to and from [illegible] computer system?

3. Write down [illegible] word pointed [illegible] to the memory word [illegible]

4. Interrupts on the [illegible] computer. A. The interrupt [illegible] B. What is stored at the [illegible] vector? C. Can an interrupt [illegible] interrupted? (yes/no) Why? D. What is the [illegible] instruction of the interrupt routine and what does it do? E. What is the last instruction of the interrupt routine and what does it do.

5. Using $2^{10} \sim 10^3$, 80 char/line, 40 line/page, 400 page/book, estimate the following: A. A mainframe hard disk holds [illegible] how many books? B. A Tape 28800 [illegible] inches long holds [illegible] how many books? C. A SSSD [illegible] floppy disk has 77 tracks [illegible] of 26 sectors (say 32) of 128 char, how many pages.

6. Add two new registers (12 bit) FRONT & REAR to the [illegible] These are pointers to a memory queue. Write the [illegible] for two new instructions. A Enqueue (op code [illegible]) puts the [illegible] AC to where REAR points and decreases [illegible] the memory contents at where FRONT points and [illegible] Include control and timing in the μ-ops.

7. Implement (ie draw circuit) of a 5-bit register [illegible] which has Two's complement control line Z.

8. If the μ-ops to the right are done in sequence [illegible] and: A. If M(7Z3H) contents is [illegible]H before this sequence, what is its contents afterwards? B. What does the sequence of μ-ops do? C. Obviously this sequence [illegible]

[illegible]

9. [illegible]

10. Explain [illegible]

AAS HW ASSIGNMENTS

CDA 4102-01 "ORG" Instructor "the good doctor" Bellenot
Office 218 Love Office Hours MW 12:30-2:15 Th 12:30-1:15

PREREQUISITES: A "C" or better in both:
COT 3132 Digital Networks
COP 3402 Ass. Lang. Prog. (or any other Ass. Lang.)

TEXTS: Main text: MANO Computer System Architecture 2nd Ed
Text: KANE 68000 Microprocessor Handbook
Sup. Notes: at Kinko or Target (Includes all TP's (see below))
Reccom: KIDDER The Soul of a new Machine

GRADES: A ≥ 90%, B ≥ 80% C ≥ 68% D ≥ 60%
Based on HW 5% (see below) TP 15% (See below)
TEST 1 20% (tentatively 7 ~~Feb~~ 85 Ch 1-6 Mano 3 Ch 1 Kane)
TEST 2 20% (tentatively 14 Mar 85 Ch 7-10 Mano Ch 2,4,5,6 Kane)
FINAL 40% (Written in Store 25 Apr 85 3-5pm) on Everything
Wed 11 Dec @ 8pm.

HW: Generally 8 or 9 problems from Mano. Assigned on Tues and due the next Tues. Late work will not be accepted. Up to 3 people can turn in the same sheet (but there must be 3 different handwritings). Each HW is graded on 0..5 scale. 2 pts for correctness of one or two problems chosen at random. 2 pts for attempting all the problems 1 pt for "presentation". HW average is computed by
min (Sum of your HW grades / 4.5 * number of HW's , 100%)

TP: A list of TP's and due date are in the sup. notes (KINKO/TARGET) These must follow different rules from HW. Graded 0..10
Rules (1) THEY MUST BE YOUR OWN WORK
Then other rules cost 1 pt each if not obeyed (*1 costs everything)
(2) Must be in INK
(3) Must be on 8½ x 11 paper
(4) Do not use both sides of a page
(5) additional pages clipped or stapled together
Late TP's will not be accepted. Your TP average is obtained by averaging the best ⅗'s of your TP scores.

CONTENT: ALL OF MANO, MOST OF KANE

graded
0

HW1 due 17 Jan 85 Ch 1 Probs 13, 14, 19 Ch 2 Probs
Ch 3 Probs 14, 16, 17

HW 2 due 21 Jan 85
Ch 2 Probs 13, 15, 17 Ch 3 Probs 21, 23, 33
Ch 4 Probs 5, 14, 16