CSC 85 FINAL 1-8 10pts each 9-16 15pts by _____

have a merry & a happy

1. In a 8-bit machine $3C_{16}$ is subtracted from BD_{16}. Give the contents of the flags C, S, V, Z and PE (parity even) after this operation.

2. A cache has an access time of 100 ns, main memory's access time is 400 ns. 80% of the references are reads (90% hit the cache, the misses access main memory after trying the cache) Writes are write through done in parallel.
   A. Compute the average access time;

   BC Suppose the hit percent is way too high. Find the hit percent where the average access is that of main memory (i.e. 400 ns)

3. The amount of information in human DNA is roughly equivalent to the information in a bookcase of books. Figuring 8 shelves to a bookcase, 128 books per shelf, 512 pages per book, 2 columns/page, 128 lines of 64 chars/column.
   A. figuring 8 bits/char how many bits of info is this as a power of two?

   BC. Using $2^{10} = 10^3$ and the old saying "9 minutes pleasure, 9 months pain" compute the baud rate of sex in Mbaud. (use 8 minutes instead of 9)

4. Write down a sequence of µ-ops (S/W for something like the ch5 computer) which exchange the contents of $M(123_H)$ and $M(ABC_H)$ (you may destroy the contents of AC) in as few clock cycles as possible

5. A Write down a sequence of assembly statements for ch. 5 chapt 5 computer which will do the same thing as problem 4 i.e. swap the contents of $M(123_H)$ and $M(ABC_H)$. Use as little extra storage is possible

   B. How many clock cycles are need to run your program?
   C. If the clock runs at 5 MHz, how many µsec are needed to run your prog?

6. A slave is being sent data from the master. List the sequence of events
   A. if 1-wire strobe control is used.

   B if 2-wire handshaking is used.

7. Carefully "step by step" illustrate the restore method when $B = 11_2$ is divided into $AQ = 0111_2$. Label what you are doing & indicate the quotient & remainder (show contents: EAQ, SC, DVF, etc.)

8. Ch 5 I/O complete the tables (CPU is never the correct answer)

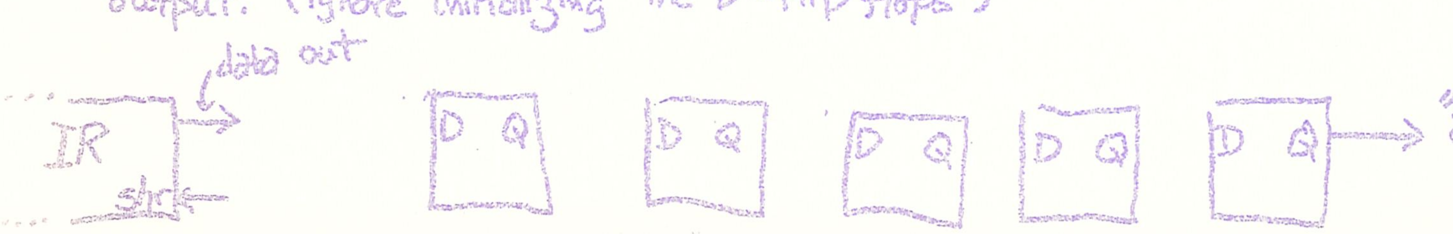
FGI was	FGI is now	data sent from	data arrived at
0	1		
1	0		

FGO was	FGO is now	data sent from	data arrived at
0	1		
1	0		

9. Write the execution cycle (complete with controls) for a memory reference instruction (opcode r) TEST_AND_SET which AC ← M[effective address] and M[effective address] ← $FFFF_H$ (note AC ← $FFFF_H$ is NOT valid for Ch 5 computer!)

10. B and T are 8-bit registers. The μ-op t: shr(T) is executed frequently but not every clock cycle. When T is "emptying" its last bit the contents of B is transfered to T. (ie t: if "T is going to be empty" then T←B) The data in B is arbitrary (any pattern). T is loaded again as the 8th bit is shifted out. A three bit register C is available. Draw a block diagram which implements these aims

11. (bit oriented protocal: zero insertion) The "infinite reg" IR contains the raw data to be sent via the zero insertion protocol. Use the 5 D flip-flops so that the line "a" sends the correct "cooked" output. (ignore initializing the D-flip flops)



FINAL #3

12. (μ-code) The Jazzed Up Chapter 8 computer is improved to include SP (stack pointer register which points to TOS and "grows" toward low memory) and the μ-code format is expanded to include F4 (see →) Op codes 9 and 12 are for CALL and RETURN. Write these in the Ch. 8 style, give ORG and worry about effective addresses

A CALL

B RETURN

F4	
0	NOP
1	SPTAR
2	INCSP
3	DECSP
4	BRTSP
5	PCTSP
6	SPTPC
7	

13. (addressing modes) The test 2 computer is a 13-bit machine with four 13-bit registers (cleverly named) R0, R1, R2 & R3 The general format for an instruction is

op-code 7 = move	source mode	source reg.	destination mode	dest. reg.
3	3	2	3	2

op-code '7' is for "move" or more correctly "copy". The "modes" are as follows note for mode = 0 the reg. field doesn't pick a reg but the reg field picks one of the "ext. modes"

mode	
0	memory reference
1	reg direct
2	reg indirect
3	index
4	pre-decrement
5	post-increment

reg (memory reference)

0	immediate
1	direct
2	indirect
3	relative

Given the instruction at M[0] is the one given below and M[1] contains 'x', M[2] contains 'y' (where addition constants and/or addresses are found) Write the effect of each instruction "á la" M[M[R0+x+M[y]]] ← R2+y"

	OP	SM	SR	DM	DR
A	7	0	0	1	3
B	7	2	2	0	1
C	7	0	3	4	1
D	7	5	0	0	2
E	7	3	2	3	3

14. Discribe the states (name & function) of the ch. 5 computer (i.e) and give the transistions (when & where)

15. Compare & contrast
A. virtual vs transparent

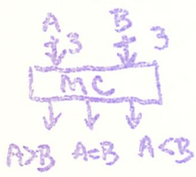
B. micocode vs hard wired logic

C. Dirty vs Valid bits

D. I/O interrupt vs internal interrupt (like ÷0)

E. Disk vs Drum

16. LRU: the numbers 0..7 are used in some sort of sequence (repetitions allowed) reg's R0..R7 contain the relative position i.e. if Ri contains 0, i was the most recently used and if Ri = 7 then i is the least recently used. R0..R7 are 3-bits wide and have INCR and CLEAR controls. The number is input on the lines $n_2\ n_1\ n_0$. You also have 8. Manitude comparers (MC) like



draw a block diagram.

Designing a digital bicycle speedometer: The idea is to count revolutions of the front wheel (in rev/sec) and translate this into speed (in mph). The equation $r = 13s$ is helpful, where r = number of revolutions of front wheel per second and s = speed in miles per hour.

A. Assume the register AR contains the number of revolutions in the last second. If speeds of at least 100 mph need to be accurately read, how wide must AR be? _____

BC. Assume the register C contains the total number of revolutions since the speedometer was last turned on. If distances of at least 1000 miles need to be accurately reported, how wide must C be? _____

D. To get the correct value in AR from the value in C we add registers OC (old C) and ROC (Real Old C) the same width as AR. Assume the control line p is "1" for exactly 1 clock cycle per second, then the micro-op p: ROC ← OC, OC ← C (the correct number of low order bits) is ~~done~~ added to the system. Explain how the value for AR can be obtained.

EFG Draw a block diagram of the system so far (when do you load AR?)

HI A "look up" table is used to translate the value in AR to the correct output codes to display the current speed. The output display has 3 digits (like 37.2) and each digit is displayed by a 7-segment display unit (decimal point is always on) What size (ie $2^n \times m$) ROM is needed? _____

JK. We are almost done with output, but the display units use too much of the battery an so we need a control line q which is "1" for exactly 1 clock cycle some where between 50 and 100 times a second. The clock rate is 1 Mega Hz and we add another register D with μ-op 1: D ← D+1 and let q be the boolean value of (D=0). Find the width of D _____
(Values somehow will only be displayed when D=1, saving lots of current (i.e. battery juice))

ORG P5

LMI: Finally we start on input. A tiny magnet is put on one spoke of the front wheel and a magnetic sensor is placed on the front fork. Spinning the front wheel, we find that the sensor "feels" the magnetic field for 1/32 of every rotation of the wheel. The clock rate is 1 MHz, how many clock pulses does the sensor "feel" the magnetic field each revolution if the bike is going 100 mph? _____ if the bike is going 1 mph? _____

OP If the sensor sends "logic 1" to the speedometer when it "feels" the magnetic field and "logic 0" otherwise, This input is serially loaded into the register IR which is four bits wide. label the sensor output line MS (magnetic sensor) write the μ-op which does this and include "control" part in the μ-op.

QRSTUVWXY:

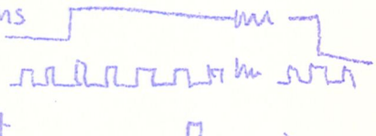
Draw a circuit which translates the "leading edge" of MS into a 1 clock pulse long output (i.e. so that out: C ← C+1 keeps the correct count of the number of revolutions)

once Q=1 & IR=1111 ~~[illegible]~~

~~[illegible]~~

OUT is "1" for one clock cycle then ~~[illegible]~~ Out is zero until the next leading edge

Note that



Za: There are 2 states (Q=0) and (Q=1) describe what each is looking for

(Q=0):

(Q=1):

b: Now we are ready to initialize the speedometer, which of our registers need to be initialized (AR, C, OC, ROC, D, IR) if we don't care if it gives incorrect ~~results~~ speeds ~~for~~ or distances for 30 secs or so but it needs to be correct after 1 min of operation.

cd How would you initialize the value of C?

[illegible] is hardware

B. Software is generally faster than hardware

C. Hardware is easier to modify than ~~hardware~~ software

D. micro-programming is an example of software taking over a function that was originally only done in hardware

E. The 68000 is "hard wired" that is it doesn't have a micro-coded controller (i.e. no micro programming)

2. On an 8-bit micro the values DF_H and 61_H are added what is the contents of the flags C, S, Z, V, PE (parity even) after this operation

C = S = Z = V = PE =

3. AB Formulate a mapping process from (macro) op-codes to (μ) control memory addresses given that μ-memory has 512 words, op-codes are 5-bits wide and 8 control words are needed for each macro-op

C. Illustrate your map with the op-code 24_{10}, give the address in BINARY

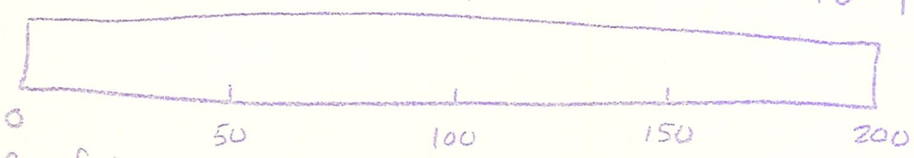
4. A. Using an Asynchronous communication with ASCII + parity + two framing bits 2400 baud is how many characters per second?

B. Compute the average access time. Cache access 100ns, Main memory 800ns, 70% are reads (80% hit cache, the misses access main memory after trying cache). Writes are write through done in parallel

C. Write down a sequence of [illegible] operations (for say, something like the [illegible] computer) which will [illegible] the memory word [illegible] the address [illegible] the memory [illegible] [illegible]

7. At time t=0 a 68000 is working on a user program A, which needs a total of 100 units of service time. The following interrupts occur (see table to right) Complete the diagram to show what the 68000 is doing at each time t

time	device	priority	service time
25	W	3	10
50	X	3	25
60	W	3	10
70	Y	5	30
90	Z	6	25



8. Carefully "step by step" illustrate the restore method when $B = 11_2$ is divided into $AB = 0100_2$ Label what the steps are doing & indicate quotient & remainder. (Show contents EAQ, SC, ...)

9. Describe the states (ie $c_0 - c_3$) of the chapter 5 computer and the state transitions (when it goes where)

10. A 12-bit SP (stack pointer) register has been added to the Chapt 5 computer, SP points to Top of Stack and grows toward low memory. Your task is to write the execution cycles (with controls for CALL (op code r) and RETURN (op code s.)

A CALL

B RETURN

11. A master device wants data from a slave device
AB List the sequence of events for 1-wire strobe control

CD List the sequence of events for 2-wire handshaking control

E. Why would you might need the cost of the extra wire in the 2-wire control (i.e. what do you gain)

12. Write μ-code in the Chapt 8 style which does M ← M+AC
The value of AC does NOT change. To start off correctly worry about effective addresses.

13. Addressing formats, describe where the operands are, or can be for ADD
A. 0-address machine
B. 1-address Machine
C. 2-address Machine
D. 3-address Machine

14. Describe how the Address of the operand is compute in each of the following addressing modes. The constant included in the instruction is C.
A. Immediate
B. Direct
C. Indirect
D. Register X indirect
E. Relative
F. Indexed by register Y
G. Register Z
H. Relative with index W and displacement

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→ out

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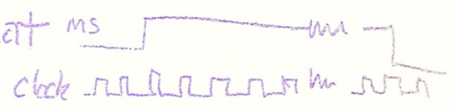

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